L Number	Hits	Search Text	DB	Time stamp
1	156920	"MAP" or (maximum adj "A" adj posteriori) or turbo or SISO or (modified adj viterbi)	USPAT; EPO; DERWENT	2003/10/28 12:33
2	20271	((look adj up) or lookup) with (entries or index or values or fields or interval)	USPAT	2003/10/28 12:10
3	887	("MAP" or (maximum adj "A" adj posteriori) or turbo or SISO or (modified adj viterbi)) with (((look adj up) or lookup) with (entries or index or values or fields or interval))	USPAT	2003/10/28 12:09
4	2448	((look adj up) or lookup) with ((plural$3 or second or two) near4 (entries or index or values or fields or interval))	USPAT	2003/10/28 12:10
5	1457	("MAP" or (maximum adj "A" adj posteriori) or turbo or SISO or (modified adj viterbi)) near4 decod$3	USPAT	2003/10/28 12:11
6	1	(("MAP" or (maximum adj "A" adj posteriori) or turbo or SISO or (modified adj viterbi)) near4 decod$3) with (((look adj up) or lookup) with ((plural$3 or second or two) near4 (entries or index or values or fields or interval)))	USPAT	2003/10/28 12:11
7	1	(("MAP" or (maximum adj "A" adj posteriori) or turbo or SISO or (modified adj viterbi)) near4 decod$3) same (((look adj up) or lookup) with ((plural$3 or second or two) near4 (entries or index or values or fields or interval)))	USPAT	2003/10/28 12:11
8	67	(("MAP" or (maximum adj "A" adj posteriori) or turbo or SISO or (modified adj viterbi)) near4 decod$3) and (((look adj up) or lookup) with ((plural$3 or second or two) near4 (entries or index or values or fields or interval)))	USPAT	2003/10/28 12:11
9	69	("MAP" or (maximum adj "A" adj posteriori) or turbo or SISO or (modified adj viterbi)) with (((look adj up) or lookup) with ((plural$3 or second or two) near4 (entries or index or values or fields or interval)))	USPAT	2003/10/28 12:14
10	162	(((look adj up) or lookup) with ((plural$3 or second or two) near4 (entries or index or values or fields or interval))) with ((comput$5 or calculat$5) near4 (value or data or entr$3))	USPAT	2003/10/28 12:16
11	2	((((look adj up) or lookup) with ((plural$3 or second or two) near4 (entries or index or values or fields or interval))) with ((comput$5 or calculat$5) near4 (value or data or entr$3))) same ("MAP" or (maximum adj "A" adj posteriori) or turbo or SISO or (modified adj viterbi))	USPAT	2003/10/28 12:16
12	0	((((look adj up) or lookup) with ((plural$3 or second or two) near4 (entries or index or values or fields or interval))) with ((comput$5 or calculat$5) near4 (value or data or entr$3))) same (("MAP" or (maximum adj "A" adj posteriori) or turbo or SISO or (modified adj viterbi)) near4 decod$3)	USPAT	2003/10/28 12:17

13	0	((((look adj up) or lookup) with ((plural$3 or second or two) near4 (entries or index or values or fields or interval))) with ((comput$5 or calculat$5) near4 (value or data or entr$3))) and (("MAP" or (maximum adj "A" adj posteriori) or turbo or SISO or (modified adj viterbi)) near4 decod$3)	USPAT	2003/10/28 12:18
14	9	(("MAP" or (maximum adj "A" adj posteriori) or turbo or SISO or (modified adj viterbi)) near4 decod$3) same (table near4 log$7)	USPAT	2003/10/28 12:25
15	0	(("MAP" or (maximum adj "A" adj posteriori) or turbo or SISO or (modified adj viterbi)) near4 decod$3) same (table near4 (log or logaritham))	USPAT	2003/10/28 12:26
16	65	(("MAP" or (maximum adj "A" adj posteriori) or turbo or SISO or (modified adj viterbi)) near4 decod$3) same (log or logaritham)	USPAT	2003/10/28 12:26
17	5	((("MAP" or (maximum adj "A" adj posteriori) or turbo or SISO or (modified adj viterbi)) near4 decod$3) same (log or logaritham)) and lookup	USPAT	2003/10/28 12:26
18	28	(("MAP" or (maximum adj "A" adj posteriori) or turbo or SISO or (modified adj viterbi)) near4 decod$3) with (lookup or (look adj up))	USPAT; EPO; DERWENT	2003/10/28 12:34

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File 347:JAPIO Oct 1976-2003/Jun(Updated 031006)
         (c) 2003 JPO & JAPIO
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200369
         (c) 2003  Thomson Derwent
File 348:EUROPEAN PATENTS 1978-2003/Oct W03
         (c) 2003 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20031023,UT=20031016
         (c) 2003 WIPO/Univentio

Set     Items   Description
S1        111   AU=YUAN W?
S2       2728   (SOFT()DECISION? ? OR MAP OR (MAX OR MAXIM?)(3W)(APOSTERIO-
             R? OR A()POSTERIOR?) OR TURBO)(5N)DECOD?
S3          4   S1 AND S2
```

3/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015535058 **Image available**
WPI Acc No: 2003-597208/200356
XRPX Acc No: N03-475951
Turbo decoder **circuit for digital communication system, has multiplexer which selects arguments difference or its inverted value as index value, when difference is positive or negative**
Patent Assignee: SANTOSA H (SANT-I); YUAN W S (YUAN-I); ZHANG M (ZHAN-I)
Inventor: SANTOSA H; **YUAN W S** ; ZHANG M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030091129	A1	20030515	US 2001905521	A	20010712	200356	B

Priority Applications (No Type Date): US 2001905521 A 20010712
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030091129	A1		19	H04L-027/06	

Abstract (Basic): US 20030091129 A1

NOVELTY - The decoder computes logarithmic function with respect to arguments (x1,x2) derived from input data. The index value generation circuit has an adder (1006) which adds argument x1, inverted argument x2 and '1' to provide a difference of x1 and x2. A multiplexer (1016) selects difference value or its inverted value as an index value, when the difference is positive or negative.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for logarithmic function computing method.

USE - Is constructed as application specific integrated circuit (ASIC), field programmable gate array (FPGA), digital signal processor (DSP) used in digital communication system.

ADVANTAGE - The index value generation circuit simplifies the computation process and enhances the performance of **turbo decoder** . The complexity and processing time of the decoder are reduced

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of index value generation circuit.

adder (1006)
multiplexer (1016)
pp; 19 DwgNo 11/13

Title Terms: TURBO; DECODE; CIRCUIT; DIGITAL; COMMUNICATE; SYSTEM; MULTIPLEX; SELECT; ARGUMENT; DIFFER; INVERT; VALUE; INDEX; VALUE; DIFFER; POSITIVE; NEGATIVE
Derwent Class: T01; U21; U22; W01
International Patent Class (Main): H04L-027/06
International Patent Class (Additional): H03D-001/00; H04L-005/12; H04L-023/02
File Segment: EPI

3/5/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015404578 **Image available**
WPI Acc No: 2003-466719/200344
XRPX Acc No: N03-371286
LUT (look-up table) addressing scheme for turbo decoding **system involves extracting address bits from index value and using address bits to address second table**
Patent Assignee: SANTOSA H (SANT-I); YUAN W S (YUAN-I); ZHANG M (ZHAN-I)
Inventor: SANTOSA H; **YUAN W S** ; ZHANG M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030056167	A1	20030320	US 2001905661	A	20010712	200344	B

Priority Applications (No Type Date): US 2001905661 A 20010712
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20030056167 A1 19 H03M-013/00

Abstract (Basic): US 20030056167 A1
NOVELTY - The method entails generating a second table having a number of entries based on a first table. First and second data fields are then generated and an index value is computed. Address bits are extracted from the index value. The address bits are used to address the second table.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) a circuit for decoding input data; and
(b) a method in a **decoder** applying the **maximum a - posteriori** probability algorithm for computing a specific function for two argument values.
USE - For **turbo decoding** system of communication systems.
ADVANTAGE - Provides improvements to **turbo decoding** that reduces complexity of **turbo decoder** and reduces **decoder** processing time. Applies to LUTs whether scaled or not.
DESCRIPTION OF DRAWING(S) - The figure is a block diagram illustrating a complete iteration of a **decoding** operation of a **turbo decoder** .
pp; 19 DwgNo 3/13
Title Terms: UP; TABLE; ADDRESS; SCHEME; TURBO; DECODE; SYSTEM; EXTRACT; ADDRESS; BIT; INDEX; VALUE; ADDRESS; BIT; ADDRESS; SECOND; TABLE
Derwent Class: T01; U14; U21; W01
International Patent Class (Main): H03M-013/00
File Segment: EPI

3/5/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015270690 **Image available**
WPI Acc No: 2003-331619/200331
XRPX Acc No: N03-265712
Turbo decoding **method used in wireless telephone, involves generating bit decision data, until bit decision data output by constituent decoders are identical**
Patent Assignee: SANTOSA H (SANT-I); YUAN W S (YUAN-I); ZHANG M (ZHAN-I)
Inventor: SANTOSA H; **YUAN W S** ; ZHANG M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030023919	A1	20030130	US 2001905780	A	20010712	200331	B

Priority Applications (No Type Date): US 2001905780 A 20010712
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20030023919 A1 19 H03M-013/00

Abstract (Basic): US 20030023919 A1
NOVELTY - The exterior information (P1,P2) and bit decision data for each input data are generated by the constituent decoders (332,334), continuously. The generation of bit decision data is stopped, when the bit decision data output by the constituent decoders, are identical.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **turbo decoder** .
USE - For **turbo decoding** of information received by wireless telephone, pager, portable personal information device, etc.
ADVANTAGE - Enables usage of N-number of constituent decoders and thereby enables fast and highly efficient decoding, using a simple circuit.

DESCRIPTION OF DRAWING(S) - The figure shows a block diagram explaining the **turbo decoding** method.
constituent decoders (332,334)
exterior information (P1,P2)
pp; 19 DwgNo 3/13
Title Terms: TURBO; DECODE; METHOD; WIRELESS; TELEPHONE; GENERATE; BIT; DECIDE; DATA; BIT; DECIDE; DATA; OUTPUT; CONSTITUENT; DECODE; IDENTICAL
Derwent Class: U21; W01
International Patent Class (Main): H03M-013/00
File Segment: EPI

3/5/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015269711 **Image available**
WPI Acc No: 2003-330640/200331
XRPX Acc No: N03-264745
Logarithmic functions computing method in digital communication system, involves generating data field including table values computed based on argument equations and scaling table values
Patent Assignee: YUAN W S (YUAN-I)
Inventor: **YUAN W S**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030014711	A1	20030116	US 2001905568	A	20010712	200331	B

Priority Applications (No Type Date): US 2001905568 A 20010712
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030014711	A1		21	H03M-013/03	

Abstract (Basic): US 20030014711 A1
NOVELTY - A data field including several table index values selected from predetermined range of argument values, is generated. The index values are scaled using a scaling factor. Another data field including table values computed based on the logarithmic/natural logarithmic equations involving the argument values, is generated. The computed table values are then scaled by the scaling factor.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following.
(1) logarithmic functions computing circuit;
(2) data decoding circuit; and
(3) data receiver.
USE - For computing logarithmic/natural logarithmic functions in data decoding circuits (claimed) in digital communication system and wireless communication system using error correction codes.
ADVANTAGE - The scaling and decoding operations can be performed with greater efficiency.
DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of the **turbo decoder** .
pp; 21 DwgNo 13/13
Title Terms: LOGARITHM; FUNCTION; COMPUTATION; METHOD; DIGITAL; COMMUNICATE; SYSTEM; GENERATE; DATA; FIELD; TABLE; VALUE; COMPUTATION; BASED; ARGUMENT; EQUATE; SCALE; TABLE; VALUE
Derwent Class: T01; U21; W01
International Patent Class (Main): H03M-013/03
File Segment: EPI

File 348:EUROPEAN PATENTS 1978-2003/Oct W03
(c) 2003 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20031023,UT=20031016
(c) 2003 WIPO/Univentio

Set	Items	Description
S1	1978	(SOFT()DECISION? ? OR MAP OR (MAX OR MAXIM?)(3W)(APOSTERIO-R? OR A()POSTERIOR?) OR TURBO)(5N)DECOD?
S2	26399	(LOOKUP? ? OR LOOK???()UP)(3N)TABLE? ? OR LUT OR LUTS
S3	1053	N(2W)(ENTRY OR ENTRIES)
S4	29282	(SECOND? OR TWO OR 2ND OR DUAL? OR MULTIPLE OR MULTIPLICIT-??? OR PLURAL? OR SEVERAL OR VARIOUS OR DIFFERENT OR SEPARATE OR ASSORT? OR ADDITIONAL)(5N)(INDEX??? OR INDICE? ?)
S5	4745	SCALING(3N)FACTOR? ?
S6	336	S2(20N)S3:S4
S7	1	S1(S)S6(S)S5 OR S1(100N)S6(100N)S5
S8	2813	TABLE? ?(20N)S3:S4
S9	1	S1(S)S8(S)S5 OR S1(100N)S8(100N)S5
S10	10	S1(S)S8(S)SCAL??? OR S1(100N)S8(100N)SCAL???
S11	2058	S2(20N)(INDEX?? OR INDICE? ?)
S12	1	S1(S)S11(S)S5 OR S1(100N)S11(100N)S5
S13	21813	TABLE? ?(20N)(INDEX?? OR INDICE? ?)
S14	2	S1(S)S13(S)S5 OR S1(100N)S13(100N)S5
S15	1	S14 NOT S12
S16	14	S1(S)S13(S)SCAL??? OR S1(100N)S13(100N)SCAL???
S17	12	S1(S)S8
S18	16	S1(S)S5
S19	34	S10 OR S14:S18

19/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01239665
OPTIMUM TURBO DECODING ARCHITECTURE AND METHOD USING A CONSTANT OR QUASI-CONSTANT SIGNAL-TO-NOISE RATIO
OPTIMALE TURBODEKODIERUNGSARCHITEKTUR UND VERFAHREN MIT ANWENDUNG EINES KONSTANTEN ODER QUASI-KONSTANTEN SIGNAL-RAUSCHVERHALTNISSES
ARCHITECTURE ET PROCEDE DE TURBODECODAGE OPTIMAL DANS LESQUELS UN RAPPORT SIGNAL-BRUIT CONSTANT OU QUASI CONSTANT EST UTILISE
PATENT ASSIGNEE:
TELEFONAKTIEBOLAGET LM ERICSSON (publ), (213766), , 126 25 Stockholm, (SE), (Proprietor designated states: all)
INVENTOR:
SCHULIST, Matthias, Taublingstr. 33, D-91058 Erlangen, (DE)
GERSTENBERGER, Dirk, Silkeborgsgatan 56, S-164 48 Kista, (SE)
MARQUARDT, Michael, Seehofallee 20, D-22177 Hamburg, (DE)
LEGAL REPRESENTATIVE:
Mohsler, Gabriele et al (84054), Ericsson Eurolab Deutschland GmbH, Patent Department, Neumeyerstrasse 50, 90411 Nurnberg, (DE)
PATENT (CC, No, Kind, Date): EP 1190489 A1 020327 (Basic)
EP 1190489 B1 021113
WO 2000074247 001207
APPLICATION (CC, No, Date): EP 2000935061 000518; WO 2000EP4495 000518
PRIORITY (CC, No, Date): US 322169 990528
DESIGNATED STATES (Pub A): AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; (Pub B): DE; FR; GB; IT
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: H03M-013/29; H04B-007/005
NOTE:
No A-document published by EPO
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200246	994
CLAIMS B	(German)	200246	816
CLAIMS B	(French)	200246	1164
SPEC B	(English)	200246	3396
Total word count - document A			0
Total word count - document B			6370
Total word count - documents A + B			6370

...SPECIFICATION employed. The decoder input metrics are then forwarded to the turbo decoder 110 for decoding.
Unlike the conventional receiver architecture illustrated in FIG. 1, the **turbo decoder** 110 in the receiver in Fig. 3 relies on a constant or quasi-constant SNR value to support the **turbo decoding** process. The constant or quasi-constant SNR value is, in accordance with a preferred embodiment of the present invention, derived from the reference SNR value...

...then modifies the reference SNR generated by the reference SNR module 125 based on one or more factors including, but not necessarily limited to, the **scaling factor** associated with decoder input metrics generated by the demodulation unit 105, coding rate, power settings and processing gains (i.e., spreading factors used on the...

...reference SNR, for example, by a factor of 1-3 dB. The modified SNR is then forwarded from the SNR adaptation unit 315 to the **turbo decoder** 110, which uses the quasi-constant, modified SNR value to generate the decoded output sequence.
As stated, the modified SNR value is a quasi-constant...

...CLAIMS B1
1. A receiver for a telecommunication system, the receiver including
- a demodulation unit (105) capable of demodulating a received telecommunications signal and producing scaled, **decode** input

metrics,
- a **turbo decoder** (110) connected to said demodulation unit (105), wherein said **turbo decoder decodes** the received signal as a function of at least the decode input metrics, characterized in that
- said receiver further includes a signal-to-noise ratio (SNR) adaptation unit (315) connected to said **turbo decoder** (110), wherein said SNR adaptation unit is capable of modifying a constant or quasi-constant SNR value as a function of at least one of...

...scheme that was applied to a transmitted signal,
- (c) a factor based on a coding rate that was applied to said transmitted signal,
- (d) a **scaling factor** associated with said decode input metrics,
- (e) power settings associated with control and data information contained in said transmitted signal,
- (f) processing gains associated with control and data information contained in said transmitted signal, thereby generating a modified SNR value,
- said **turbo decoder** (110) **decodes** the received signal as a function of the decode input metrics and the modified SNR value.

2. The receiver of claim 1, wherein the constant...

19/3,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00991424
Start code detecting apparatus for video data stream
Vorrichtung zur Startkodedetektierung fur Videodatenstrom
Appareil de detection de code de depart pour le flux de donnees video
PATENT ASSIGNEE:
Discovision Associates, (260275), 2355 Main Street, Suite 200, Irvine, CA 92614, (US), (Applicant designated States: all)
INVENTOR:
Wise, Adrian Philip, 10 Westbourne Cottages, Frenchay, Bristol BS16 1NA, (GB)
Sotheran, Martin William, The Ridings, WickLane Stinchcombe, Dursley, Gloucestershire GL11 6BD, (GB)
Robbins, William Philip, 19 Springhill, Cam, Gloucestershire GL11 5PE, (GB)
Finch, Helen Rosemary, Tyley, Coombe, Wotton-under-edge, Gloucester GL12 7ND, (GB)
Boyd, Kevin James, 21 Lancashire Road, Bristol, BS7 9DL, (GB)
LEGAL REPRESENTATIVE:
Vuillermoz, Bruno et al (72791), Cabinet Laurent & Charras B.P. 32 20, rue Louis Chirpaz, 69131 Ecully Cedex, (FR)
PATENT (CC, No, Kind, Date): EP 896477 A2 990210 (Basic)
EP 896477 A3 990922
APPLICATION (CC, No, Date): EP 98202175 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
RELATED PARENT NUMBER(S) - PN (AN):
EP 674443 (EP 95301301)
INTERNATIONAL PATENT CLASS: H04N-007/24; G06F-013/00; G06F-009/38
ABSTRACT WORD COUNT: 95
NOTE:
Figure number on first page: 61

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9906	578
SPEC A	(English)	9906	126716
Total word count - document A			127294
Total word count - document B			0

Total word count - documents A + B 127294

...SPECIFICATION ability to take the DRAM interface to high impedance is provided to allow other devices to test or use the DRAM controlled by the Spatial **Decoder** (or the Temporal **Decoder**) when the Spatial Decoder (or the Temporal Decoder) is not in use. It is not intended to allow other devices to share the memory during...

...an interval determined by the register, refresh(underscore)interval. The value in refresh(underscore)interval specifies the interval between refresh cycles in periods of 16 **decoder** (underscore)clock cycles. Values in the range 1.255 can be configured. The value 0 is automatically loaded after reset and forces the DRAM interface...in one location and the control registers, coded(underscore)busy, enable(underscore)mpi(underscore)input and coded(underscore)extn are in a second location.

(See **Table** A.9.7).
When configured for Token input via the MPI, the current Token is extended with the current value of coded(underscore)extn each...

19/3,K/13 (Item 13 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00676530
RECEIVER FOR A DIRECT SEQUENCE SPREAD SPECTRUM ORTHOGONALLY ENCODED SIGNAL EMPLOYING RAKE PRINCIPLE
EMPFANGER FUR DIREKTSEQUENZ-SPREIZSPEKTRUM ORTHOGONAL KODIERTES SIGNAL UNTER ANWENDUNG DES "RAKE"-PRINZIPS (RECHENFORMIGER AUFBAU)
RECEPTEUR POUR SIGNAL A CODAGE ORTHOGONAL A SPECTRE ETALE A SEQUENCE DIRECTE, EMPLOYANT LE PRINCIPE DU RATEAU
PATENT ASSIGNEE:
QUALCOMM INCORPORATED, (910892), 6455 Lusk Boulevard, San Diego, California 92121, (US), (applicant designated states: AT;BE;CH;DE;DK;ES;FR;GB;GR;IE;IT;LI;LU;MC;NL;PT;SE)
INVENTOR:
VITERBI, Audrey, 8490 Whale Watch Way, La Jolla, CA 92037, (US)
VITERBI, Andrew, 2712 Glenwick Place, La Jolla, CA 92037, (US)
LEGAL REPRESENTATIVE:
Walsh, Michael Joseph et al (72431), TOMKINS & CO. 5, Dartmouth Road, Dublin 6, (IE)
PATENT (CC, No, Kind, Date): EP 705510 A1 960410 (Basic)
EP 705510 B1 980415
WO 9501018 950105
APPLICATION (CC, No, Date): EP 94921281 940622; WO 94US6602 940622
PRIORITY (CC, No, Date): US 83110 930624
DESIGNATED STATES: AT; BE; CH; DE; DK; ES; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
INTERNATIONAL PATENT CLASS: H04K-001/00; H04B-007/005;
NOTE:
No A-document published by EPO
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9816	961
CLAIMS B	(German)	9816	946
CLAIMS B	(French)	9816	1057
SPEC B	(English)	9816	7617
Total word count - document A			0
Total word count - document B			10581
Total word count - documents A + B			10581

...SPECIFICATION in coordination with the predetermined ordering scheme. Selected decision value 146 is input to metric computation mechanism 150 which scales the selected decision value to **scaling factor** 154 which can be used as a **scaling factor** in forming an individual soft

decision data which can subsequently be used in forming **soft decision** transition metrics for maximum likelihood **decoding** techniques. The index data symbol associated with selected decision value 148 is input to index mapping mechanism 152 which maps the index data symbol into...

...bit length index data symbol maps into 6 soft decision bits). Multiplier 158 multiplies each of the plurality of (+-)1 soft decision bits 156 by **scaling factor** 154 to form individual soft decision data 160 for each soft decision bit (e.g., 6 soft decision bits form 6 individual soft decision data...

19/3,K/16 (Item 3 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00977489 **Image available**
METHOD AND APPARATUS FOR EFFICIENTLY CALCULATING LOG-LIKELIHOOD RATIOS
PROCEDE ET APPAREIL DE CALCUL EFFICACE DE TAUX DE PROBABILITE
Patent Applicant/Assignee:
KONINKLIJKE PHILIPS ELECTRONICS N V, Groenewoudseweg 1, NL-5621 BA Eindhoven, NL, NL (Residence), NL (Nationality)
Inventor(s):
HE Allen, Prof. Holstlaan 6, NL-5656 AA Eindhoven, NL,
PRENTICE Andrew, Prof. Holstlaan 6, NL-5656 AA Eindhoven, NL,
Legal Representative:
MAK Theodorus N (et al) (agent), Internationaal Octrooibureau N.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven, NL,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200307529 A1 20030123 (WO 0307529)
Application: WO 2002IB2600 20020628 (PCT/WO IB0202600)
Priority Application: US 2001904355 20010712
Designated States: CN JP KR
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
Publication Language: English
Filing Language: English
Fulltext Word Count: 4004
Fulltext Availability:
Detailed Description

Detailed Description
... ij2+0j')]-EsAO[2x(ii-ij)-2y(oi-0j)] (Eq.4)
N N
Finally, the term (E,N)Ao may be accounted for in the **turbo decoder** by a
scaling factor . Preferably, however, the **turbo decoder** is based on the Max-log-MAP algorithm, which has a factor to cancel the (E,N)Ao term. Therefore, Eq. 4 becomes.

LLR(m...

19/3,K/17 (Item 4 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00973568 **Image available**
TURBO DECODER WITH MULTIPLE SCALE SELECTIONS
TURBO DECODEUR AVEC DES SELECTIONS MULTI-ECHELLES
Patent Applicant/Assignee:
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Inventor(s):
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Legal Representative:
WADSWORTH Philip R (et al) (agent), Qualcomm Incorporated, 5775 Morehouse Drive, San Diego, California 92121-1714, US,

Patent and Priority Information (Country, Number, Date):
  Patent: WO 200303586 A2 20030109 (WO 0303586)
  Application: WO 2002US20345 20020626 (PCT/WO US0220345)
  Priority Application: US 2001893046 20010627
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
  (EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
  (OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
  (AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
  (EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 9747

Fulltext Availability:
  Detailed Description
  Claims

English Abstract

Techniques to improve the performance of a **Turbo decoder** when scale information for the bits in a code segment to be decoded is not known. A number of hypotheses are formed for the code segment, with each hypothesis corresponding to a particular set of one or more values for a set of one or more parameters used for **decoding** the code segment. For the **MAP decoding** scheme, these parameters may be for the sequence of **scaling factors** used to scale the bits prior to decoding and/or a scale used to evaluate a (e.g., min*) function for the **MAP decoding** . The code segment is **decoded** based on the **MAP decoding** scheme and in accordance with each hypothesis. The quality of the decoded result for each hypothesis is determined based on one or more performance metrics. The decoded bits for the best hypothesis are provided as the **Turbo decoder** output.

Detailed Description

... MAP decoding may@ degrade because the function may not be accurately evaluated.

[00121 Aspects of the invention provide techniques to improve the perforrnance of a **Turbo decoder** when the scale information for the received bits is not known. In general, a number of hypotheses are formed for a given code segment to...

...decoded, with each hypothesis h corresponding to a particular set of one or more values for a set of one or more parameters used for **decoding** the code segment. For the **MAP decoding** scheme, these parameters may be for (1) the sequence of **scaling factors** used to ...To reduce the storage requirement, the received bits
V = IV, V2 V3 0** V30 are effectively scaled via a multiplier 312 by a sequence of **scaling factors** S = {sl S2 S3 ... S30. One **scaling factor** may be provided for each received bit vk, and the scaling may be performed element by element for the sequence V. The scaled bits are then quantized by a quantizer 314 to provide the decoder input bits U = ju, U2 U3 0** U3N I. The input bits Uk to the **Turbo decoder** are thus scaled and quantized version of the received bits vk and may have a reduced resolution (e.g., of 4, 5, 6, or some...of a scaled bit can be expressed as.

2
Wk = Sk k
Ak
where wk represents the "scale" of the input bit Uk into the **MAP decoder** . The **scaling factor** Skis typically selected for each received bit Vk in the code segment
U2
such that the quantity 'Sk k / Ak for all scaled bits Uk are approximately equal (i. e., wk= w for a given code segment). Various

are derived by scaling received bits with a sequence of **scaling factors** , and wherein the plurality of hypotheses correspond to a plurality of sequences of **scaling factors** .

19/3,K/18 (Item 5 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00939749 **Image available**
WIRELESS COMMUNICATIONS METHODS AND SYSTEMS FOR LONG-CODE AND OTHER SPREAD SPECTRUM WAVEFORM PROCESSING
SYSTEMES ET PROCEDES DE COMMUNICATIONS SANS FIL POUR LE TRAITEMENT DE FORMES D'ONDE A ETALEMENT DU SPECTRE ET DE FORMES D'ONDE LONG CODE
Patent Applicant/Assignee:
MERCURY COMPUTER SYSTEMS INC, 199 Riverneck Road, Chelmsford, MA 01824, US, US (Residence), US (Nationality)
Inventor(s):
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Legal Representative:
POWSNER David J (et al) (agent), Nutter, McClennen & Fish LLP, One International Place, Boston, MA 02110-2699, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200273937 A2-A3 20020919 (WO 0273937)
Application: WO 2002US8106 20020314 (PCT/WO US0208106)
Priority Application: US 2001275846 20010314; US 2001289600 20010507; US 2001295060 20010601
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 149462

Fulltext Availability:
Detailed Description

Detailed Description
... of the processing requirements.

If a particular data user is to be processed with an 80+ ms, latency 804 so as to include the full **turbo decode** within the MUD loop then the input channel bit-error rate (BER) pertainI 0 ing to these users might be extraordinarily high. Here, the MUD...

...Each box is the same code but configured differently. The parameters that differ are.
N-FRAMES-RAKE-OUTPUT;
Decoding to be performed (e.g. repetition **decoding** , **turbo decoding** , and the like);
Classes of users to be cancelled;
Threshold parameters.

The pseudo code for the software implementation of one long-code multiple user detection...

...physical users
Read
in
rake
outpu@
records (N frames)
Refonnat-rake-output-data (N frames at a time)

for stage = 1 : N-stages
Perform appropriate **decoding** (SRD, **turbo** , and the like, depending on TTI)
Perfon-n-long
code-mud
1 5 end
Free memory
The following four functions are described below.

Read-in-rake-OutpuLrecords;
Reformat-rake-outpuLdata
Perform appropriate **decoding** (SRD, **turbo** , and the like, "depending on TTI);
Perf6nn
long
@code
mud.

The Read-in-rake-output-records function performs.

Reading in data for each user; and...BITS-PER-FRAME-1 150*4.25 640.

Each user class has a specified decoding to be performed. The decoding can be.

None
Soft Repetition **Decoding** (SRD)
Turbo **decoding**
Convolutional **decoding** .

All **decoding** is Soft-Input Soft-Output (SISO) decoding. For example, an SF 64 voice user produces 600 soft bits per frame. Thus 1,200 soft bits ...and the operation can be performed in-place. If further decoders are included, reduced complexity partial-decode variants can be employed to reduce complexity. For **turbo** **decoding** , for example, the number of iterations may be limited to a small number.

42
The Long-code MUD performs the following operations.

Respread
Raised-Cosine...software exception was detected) (RIW local)
3 RESETREQjN Wrap status of the local CPU's reset request
4 WDM-INIT WDM failed in initial 2 **second** window (0 = WDM failed)
5 Software definable 0 Software definable 0
6 Software definable 1 Software definable I
7 unused unused
Table 8. Fault Status Register Format
Bit Name, Description
0 RESETREQ-OUT-0 Request a reset event (O => forces reset)
I CHKSTOPOUT 0 Request that node...

19/3,K/19 (Item 6 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00920500 **Image available**
CHANNEL CODEC PROCESSOR CONFIGURABLE FOR MULTIPLE WIRELESS COMMUNICATIONS STANDARDS
PROCESSEUR CODEC DE VOIES CONFIGURABLE POUR DES COMMUNICATIONS SANS FIL MULTIPLES
Patent Applicant/Assignee:
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Inventor(s):
BITTERLICH Stefan Johannes, 675 Campbell Technology Parkway, Suite 100, Campbell, CA 95008, US,

HOLMES David Morris, 21696 Noonan Court, Cupertino, CA 95014, US,
Legal Representative:
MORRIS Frank E (et al) (agent), Pennie & Edmonds LLP, 1155 Avenue of the Americas, New York, NY 10036, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200254601 A1 20020711 (WO 0254601)
Application: WO 2001US49478 20011228 (PCT/WO US0149478)
Priority Application: US 2000258865 20001229
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 10922

Fulltext Availability:
Detailed Description

Detailed Description
... programmable code rate.

user programmable constraint length.

user programmable code.

reconfigurable convolutional encoders.
user programmable code rate.

user programmable constraint length.

user programmable code.

reconfigurable **Turbo** **Decoders** (based on log- **MAP** [**Maximum** - **A** - **Posterioril**)
user programmable maximum number of iterations.

user programmable energy pre- **scaling** .

user programmable iteration termination condition(s).

reconfigurable Turbo Encoders.

reconfigurable CRC Generators / Checkers,
user programmable generator polynomials.

Rate-matching **index** generators,
a user programmable **index** update parameters.
Puncturing/depuncturing support.

Interleaver and deinterleaver address generators
table -based,
user programmable algorithm selection: Max-Log-MAP or Log-MAP algorithm,
or algorithm based (the algorithms used in the 3rd generation wireless standards are supported in hardware to minimize power consumption and **table** size).

Block segmentation/concatenation HW support
0 User programmable **index** update parameters.

0 User programmable length parameters with associated selectable micro-interrupt capabilities,
User programmable simultaneous Bit-Segmentation/Bit-concatenation

support.

Reed-Muller Coder for...

19/3,K/20 (Item 7 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00903554 **Image available**
METHOD OF PERFORMING HUFFMAN DECODING
PROCEDE DE DECODAGE DE HUFFMAN
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Patent Applicant/Inventor:
ACHARYA Tinku, 4840 West Erie Street, Chandler, AZ 85226, US, US (Residence), IN (Nationality), (Designated only for: US)
TSAI Ping-Sing, 420 West Desert Avenue, Gilbert, AZ 85233, US, US (Residence), US (Nationality), (Designated only for: US)
Legal Representative:
MALLIE Michael J (agent), Blakely Sokoloff Tayolor & Zafman, 7th Floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (et al), US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200237687 A2-A3 20020510 (WO 0237687)
Application: WO 2001US31532 20011009 (PCT/WO US0131532)
Priority Application: US 2000704380 20001031
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 3821

Fulltext Availability:
Detailed Description

Detailed Description
... of a Huffman encoding table with the corresponding decoding tree. One problem associated with such a decoder in hardware or software is how to efficiently **map** the **decoding** tree into memory. For example, FIG. 5 illustrates a table of read only memory (ROM) entries for bit serial Huffman decoding using the decoding tree...

...memory was proposed for example, by Mukherjee et al., "MARVLE: a VLSI chip for data compression using tree-based codes," IEEE Transactions on Very Large **Scale** Integration (VLSI) System, 1(2):203-214, June 1993.

Another approach, although not particularly efficient, for decoding the Huffman code, is to compare each entry of the Huffman **table** with input bits in the input buffer. Under this approach, at worst, **N** **entries** in the encoding **table** will be
7
compared, where N is the total number of symbols. In addition, the code length information for the entry is to be known...

19/3,K/21 (Item 8 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00897761 **Image available**

IMPROVED DECODING OF TURBO CODES USING DATA SCALING
DECODAGE AMELIORE DE CODES TURBO PAR MISE A L'ECHELLE DE DONNEES

Patent Applicant/Assignee:
MOTOROLA INC, 1303 East Algonquin Road, Schaumburg, IL 60196, US, US (Residence), US (Nationality)
Inventor(s):
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Legal Representative:
VAAS Randall S (et al) (agent), Motorola, Inc., 600 North U.S. Highway 45, Libertyville, IL 60048, US,

Patent and Priority Information (Country, Number, Date):
Patent: WO 200231964 A1 20020418 (WO 0231964)
Application: WO 2001US42450 20011002 (PCT/WO US0142450)
Priority Application: US 2000686575 20001011
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 4055

Fulltext Availability:
Detailed Description

English Abstract
A method (100) for improved decoding of received convolutionally coded input data uses data scaling to provide near ideal **turbo decoding** . The method includes a first step of loading (102) a portion of the input data into a buffer. A next step includes calculating (104) a...

...root-mean-square value of the portion of the input data using the mean from the calculating step. A next step includes deriving (108) a **scaling factor** from the root-mean-square value of the computing step, and a next step includes scaling (110) the portion of input data by the **scaling factor** of the deriving step.

Detailed Description
... the mean is taken over the symbols in the frame. Each symbol is then scaled by the computed frame RMS, before being passed to the **turbo decoder** , as represented in FIG. 6. In other words, the entire frame is scaled the same amount. The **scaling factor** is computed as follows.

K C (14)
RMS
N 2
-2
E Y" Y
n

Empirical study has shown that a value of about four...shows a flow chart representing a method 1 00 for improved decoding of received convolutionally coded input data uses data scaling to provide near ideal **turbo decoding** . The method includes a first step of loading 102 a portion of the input data into a buffer. Preferably, the portion is a frame of...

...root-mean-square value of the portion of the input data using the mean from the calculating step. A next step includes deriving 108 a **scaling factor** from the root-meansquare value of the computing step, and a next step includes scaling 1 1 0 the portion of input data by the **scaling factor** of the deriving step. The scaled data is then sent to the **turbo decoder** for **decoding** .

In a preferred embodiment, the above steps are repeated until all the

input data is decoded. In addition, the calculating step includes calculating a symbol...

19/3,K/22 (Item 9 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00855408 **Image available**
FRAME CONTROL ENCODER/DECODER FOR ROBUST OFDM FRAME TRANSMISSIONS
CODEUR/DECODEUR DE COMMANDE DE TRAME POUR TRANSMISSIONS DE TRAMES A MULTIPLEXAGE FREQUENTIEL ORTHOGONAL
Patent Applicant/Assignee:
INTELLON CORPORATION, 5100 West Silver Springs Boulevard, Ocala, FL 34482 , US, US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
YONGE Lawrence W III, 5100 West Silver Springs Boulevard, Ocala, FL 34482 , US, US (Residence), US (Nationality), (Designated only for: US)
Legal Representative:
LEE G Roger (agent), Fish & Richardson P.C., 225 Franklin Street, Boston, MA 02110-2804, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200189124 A1 20011122 (WO 0189124)
Application: WO 2001US40777 20010518 (PCT/WO US0140777)
Priority Application: US 2000574959 20000519
Parent Application/Grant:
Related by Continuation to: US 2000574959 20000519 (CON)
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 14587

Fulltext Availability:
Detailed Description

Detailed Description
... 64
and -64 representing the ideal values, that is, a binary 1 and a binary 0, respectively. The 100 soft values are received by the **turbo** product **decoder** 182, which performs a **turbo** (iterative) **decoding** process on each set of horizontal code words and each set of vertical code words of the product code block to produce the original 25...
...decoding (step 196), decodes each of the columns (step 198) and scales the output of the column decoding (step 200). Thus, each iteration of the **turbo** product **decoding** process includes **decoding** each of 10 rows followed by decoding each of the 10 columns and, after row or column decoding, the lo values may be scaled as necessary to adjust the precision to the full precision of the memory. A **scaling** by a **factor** of 2 (inverted exclamation mark)s
applied to all elements of the 10x10 matrix when the maximum element has a value of less than half...

19/3,K/23 (Item 10 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00853134 **Image available**

SCALED-FEEDBACK TURBO DECODER
DECODEUR TURBO A RETROACTION ECHELONNEE

Patent Applicant/Assignee:
NOKIA NETWORKS OY, Keilalahdentie 4, FIN-02150 Espoo, FI, FI (Residence), FI (Nationality)
NOKIA INC, 6000 Connection Drive, Irving, TX 75039, US, US (Residence), US (Nationality), (Designated only for: LC)
Inventor(s):
HEINILA Marko, Pajalahdentie 17 F 111, FIN-00200 Helsinki, FI,
Legal Representative:
STUART Michael C (agent), Cohen, Pontani, Lieberman & Pavane, Suite 1210, 551 Fifth Avenue, New York, NY 10176, US,

Patent and Priority Information (Country, Number, Date):
Patent: WO 200186822 A1 20011115 (WO 0186822)
Application: WO 2001IB246 20010223 (PCT/WO IB0100246)
Priority Application: US 2000565502 20000505
Designated States: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 4410

Fulltext Availability:
Detailed Description

Detailed Description

... single-processor embodiment of Fig. 5 is thus preferable for incorporation in an application-specific integrated circuit (ASIC).

Fig. 6 depicts the form of a **Turbo decoder** incorporating feedback scaling according to the present invention. Coding gain is improved by scaling the feedback in a **Turbo decoder** . The difference shown in Fig. 6 over the corresponding Fig. 2 of the prior art is the addition of multipliers 610 and 620, which scale each soft-bit number at the decoder cutputs by the **scaling factor** S (the same value of S on both multipliers) Positive results are obtained with values of S that are less than 1. Best results have...

...as improved by the present invention. Multipliers 710 and 720 are introduced for scaling the feedback signals (outputs of summers 324 and 354) by a **scaling factor** . Also, the present invention enables the replacement of decoders 318 and 348 (which, as noted above, employ the log **MAP** algorithm), with **decoders** 718 and 748 which employ the simpler max log MAP algorithm. Without the invention, there is a degradation in performance if the max log MAP...

...of Fig. 5 as improved by the present invention. Multiplier 810 is introduced for scaling the feedback signal (output of summer 440) by a **scaling factor** . **Decoder** 422 (employing the log **MAP** algorithm) can now be replaced by decoder 822 which employs the simpler max log **MAP** algorithm. As explained above, **decoder** 822 functions alternatively as first decoder 111A and second decoder 11IB of Fig. 6.

Accordingly, multiplier 810 functions alternatively as multipliers.610 and 620 of Fig. 6.

Fig. 9 is a plot of simulation results of Frame
Error Rate vs. number of **decoding** iterations using the **Turbo** **decoder** of the present invention with several different **scaling** **factors** and assuming a signal with additive white Gaussian noise (AWGN), Eb/No of 1.0 db., ...K = 4, and a transmission of 10000 frames. It (inverted exclamation mark)S desirable to lower the frame error rate, indicating fewer errors in transmission. **Scaling** **factors** used are 1.0, 0.8, 0.7, and 0 (A **scaling** **factor** of 1.0 is tantamount to not using the scaling taught by the invention.) Fig. 9 shows that a FER of 0.01, for example, (meaning that one frame out of a hundred is received with an error) may be attained after 14 **Turbo** **decoding** iterations with a **scaling** **factor** of 1.0 ((inverted exclamation mark).e., without using the scaling of the invention), after 7 iterations with a **scaling** **factor** of 0.6, and after 6 iterations with a **scaling** **factor** of 0.7 or 0 Thus, the present invention provides a reduction from 14 iterations to 6 to achieve a particular FER. This enables a substantial increase in speed if a single processor **Turbo** **decoder** is used, and a substantial increase in speed and a substantial reduction in hardware if a pipelined **Turbo** **decoder** is used.

Fig. lo is a plot of simulation results of FER vs. Eb/No using the present invention with several different scaling factors and...

19/3,K/24 (Item 11 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00846505 **Image available**
IMPROVED READ/WRITE CHANNEL
CANAL DE LECTURE/ECRITURE AMELIORE
Patent Applicant/Assignee:
INFINEON TECHNOLOGIES NORTH AMERICA CORP, 1730 North First Street, San Jose, CA 95112, US, US (Residence), US (Nationality)
Inventor(s):
RAE James Wilson, 1979 Waterford Place SW, Rochester, MN 55902, US,
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ASHLEY Jonathan, 460 Monterey Avenue, Los Gatos, CA 95030, US,
KARABED Razmik, 797 Honeywood Court, San Jose, CA 95120, US,
FRANCK Stephen J, 6633 Cooper Street, Felton, CA 95018, US,
MISTLEBERGER Fritz, Suedmaehrerweg 1, 85368 Moosburg, DE,
DRILLER Matthias, 103 Idaho Avenue, Santa Cruz, CA 95062, US,
STOCKMANS Heiner, 355 Western Drive Apt. L, Santa Cruz, CA 95060, US,
MARGRAF Dominik, 117 Felix Street #14, Santa Cruz, CA 95060, US,
Legal Representative:
GOREN David J (agent), Fish & Richardson P.C., 2200 Sand Hill Road #100, Menlo Park, CA 94025, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200180238 A1 20011025 (WO 0180238)
Application: WO 2001US11399 20010405 (PCT/WO US0111399)
Priority Application: US 2000194954 20000405
Designated States: CN JP SG
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
Publication Language: English
Filing Language: English
Fulltext Word Count: 45197

Fulltext Availability:
Claims

Claim

.'.. v'oltage divided by RMS noise voltage.
8w6m2 OffmTrack Interference-Emulator
The input to the Viterbi detector prefilter can be artificially corrupted by adding a **scaled** output from-a linear feedback shift register (LFSR). Th@ amplitude of the LFSR can be varied 'by register 75<7:0>. The frequency content of...

...to the Viterbi detector prefilter is measured by comparing input amplitude samples.to the known-data pattern. The derived error signal is multiplied by a **scaling factor** and then adided back to the known signal. This uniformly muitiplies afl noises and distortions by the **scaling factor** , creati'ng a uniform degradation of the effective detector SNIR. The amplitude of the noise multiplication error is adjPsted by register 75<7:0>.
8...111 x 0 0 NSYNC Not sync-byte found
111 0 1 x WRITE-ERROR WRITE error
111 0 0 1 1 GRAY-DATA GRAY **decode** output
126
Register **Map**
9.1 Register Map **Index**
Table 25 Register Map Group Assignments
Group Address Range Description
0000 00 - 07 Power and Mode Control
00001 08 - OF Counter Timers
00010 10 - 174 ITIR...

19/3,K/25 (Item 12 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00811803 **Image available**
VIDEO, AUDIO AND GRAPHICS DECODE, COMPOSITE AND DISPLAY SYSTEM
SYSTEME COMPOSITE DE PRESENTATION A DECODAGE VIDEO AUDIO ET GRAPHIQUE
Patent Applicant/Assignee:
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Patent Applicant/Inventor:
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Patent and Priority Information (Country, Number, Date):
Patent: WO 200145426 A1 20010621 (WO 0145426)
Application: WO 2000US33757 20001213 (PCT/WO US0033757)
Priority Application: US 99170866 19991214; US 2000641374 20000818; US 2000641936 20000818; US 2000643223 20000818; US 2000640870 20000818; US 2000640869 20000818; US 2000641930 20000818; US 2000641935 20000818; US 2000642510 20000818; US 2000642458 20000818
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ

LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG
SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
((OAPI utility model)) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 85836

Fulltext Availability:
Detailed Description

Detailed Description
... and location on the screen,
allowing the creation of solid color windows with any size and
23
location. Thus, in the preferred embodiment, no pixel **map** is
required, memory bandwidth requirements are reduced and a window
of any size may be displayed.

Another type of graphics window that the window descriptors...format,
using one of the multiple formats allowed in the
present invention and specified in the window descriptor. Each
pixel may occupy as little as **two** bits or as much as 16 bits in
the preferred embodiment. Each pixel is converted to a YUVa24
format (also referred to as aYUV 4...

19/3,K/26 (Item 13 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00760935 **Image available**
APPARATUS AND METHOD FOR ADAPTIVE MAP CHANNEL DECODING IN RADIO TELECOMMUNICATION SYSTEM
APPAREIL ET PROCEDE DE DECODAGE DE VOIE ADAPTATIF "MAP" DANS UN SYSTEME DE TELECOMMUNICATION RADIO
Patent Applicant/Assignee:
SAMSUNG ELECTRONICS CO LTD, 416, Maetan-dong, Paldal-gu, Suwon-shi, Kyungki-do 442-370, KR, KR (Residence), KR (Nationality)
Inventor(s):
KIM Beong-Jo, Mujigaemaeul #201, Kumi-dong, Puntang-gu, Songnam-shi, Kyonggi-do 463-500, KR
KIM Min-Goo, 973-3, Youngtong-dong, Paltal-gu, Suwon-shi, Kyonggi-do 442-470, KR
Legal Representative:
LEE Keon-Joo, Mihwa Bldg. 110-2, Myongryun-dong 4-ga, Chongro-gu, Seoul 110-524, KR
Patent and Priority Information (Country, Number, Date):
Patent: WO 200074399 A1 20001207 (WO 0074399)
Application: WO 2000KR554 20000529 (PCT/WO KR0000554)
Priority Application: KR 9919476 19990528
Designated States: AU BR CA CN IN JP
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Filing Language: English
Fulltext Word Count: 6131

Fulltext Availability:
Detailed Description

English Abstract
An adaptive **MAP** channel **decoding** apparatus and method in a mobile
communication system. In the adaptive **MAP** channel **decoding** apparatus,
a channel estimator calculates channel noise power and a **scaling
factor** , a controller determines an operation mode by checking
accumulated channel noise power and the **scaling factor** , and a **MAP**

performance of the **MAP** channel **decoder** is very sensitive to a current channel state.

On the other hand, the sub- **MAP** channel **decoder** exhibits a slow change in
decoding performance with respect to the change of the **scaling factor** g. That is, the sub- **MAP** **decoding** has a wider operation range with respect to the change of the **scaling factor** g than the **MAP** **decoding** . Accordingly, the sub- **MAP** **decoding** scheme according to the embodiment of the present invention is more stable with less influence from the current channel state in a real mobile radio environment, as compared to the **MAP** **decoding** scheme.

As shown in FIG. 3, the sub-MAP channel decoder has a stable operation range from about -100 to +100, whereas the " channel decoder channel estimator 420 calculates a channel noise power and a **scaling factor** from the output of the receiver 410. A controller 430 determines the operation mode of a **MAP** channel **decoder** between a. static channel mode and a time-varying mode according to the output of the channel estimator 420.

The determination is made based on changes in channel noise power and the **scaling factor** . The controller 430 can determine the operation mode based on BERXER received from the **MAP** channel **decoder** 440. For example, if a predetermined - 10number of successive occurrences of a scalm'g factor approximate to a predetermined dB are observed, the controller 430...

...the sub-MAP algorithm has increased stability in a real mobile communication channel environment as compared to the MAP algorithm.

In accordance with the adaptive **MAP** channel **decoding** apparatus and method of the present invention, a current channel state is first checked based on the change of accumulated channel noise power or a **scaling factor** of a channel - 12
estimator, or a change 'in BERTER of a " channel decoder. If the current channel state is determined to be static, decoding...

19/3,K/27 (Item 14 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00760801 **Image available**
OPTIMUM TURBO DECODING ARCHITECTURE AND METHOD USING A CONSTANT OR QUASI-CONSTANT SIGNAL-TO-NOISE RATIO
ARCHITECTURE ET PROCEDE DE TURBODECODAGE OPTIMAL DANS LESQUELS UN RAPPORT SIGNAL-BRUIT CONSTANT OU QUASI CONSTANT EST UTILISE
Patent Applicant/Assignee:
TELEFONAKTIEBOLAGET LM ERICSSON (publ), S-126 25 Stockholm, SE, SE (Residence), SE (Nationality)
Inventor(s):
SCHULIST Matthias, Taublingstr. 33, D-91058 Erlangen, DE
GERSTENBERGER Dirk, Silkeborgsgatan 56, S-164 48 Kista, SE
MARQUARDT Michael, Seehofallee 20, D-22177 Hamburg, DE
Legal Representative:
TONSCHEIDT Andreas, Ericsson Eurolab Deutschland GmbH, Ericsson Allee 1, D-52134 Herzogenrath, DE
Patent and Priority Information (Country, Number, Date):
Patent: WO 200074247 A1 20001207 (WO 0074247)
Application: WO 2000EP4495 20000518 (PCT/WO EP0004495)
Priority Application: US 99322169 19990528
Designated States: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG

(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 5116

Fulltext Availability:
Detailed Description

Detailed Description
... The decoder input metrics are then forwarded to the turbo decoder I 10 for decoding.

Unlike the conventional receiver architecture illustrated in FIG. 1, the **turbo decoder** I 10 in the receiver in Fig. 3 relies on a constant or quasi-constant SNR value to support the **turbo decoding** process. The constant or quasi-constant SNR value is, in accordance with a preferred embodiment of the present invention, derived from the reference SNR value...

...then modifies the reference SNR generated by the reference SNR module 125 based on one or more factors including, but not necessarily limited to, the **scaling factor** associated with decoder input metrics generated by the demodulation unit 105, coding rate, power settings and processing gains (i.e., spreading factors used on the...

...reference SNR, for example, by a factor of 1-3 dB. The modified SNR is then forwarded from the SNR adaptation unit 315 to the **turbo decoder** I 10, which uses the quasi-constant, modified SNR value to generate the decoded output sequence.

As stated, the modified SNR value is a quasi...

19/3,K/28 (Item 15 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00757425 **Image available**
SYSTEM AND METHOD FOR THE DEMODULATION OF TURBO-ENCODED SIGNALS VIA PILOT ASSISTED COHERENT DEMODULATION
SYSTEME ET PROCEDE DE DEMODULATION DE SIGNAUX TURBO-CODES PAR DEMODULATION COHERENTE ASSISTEE PAR PILOTE
Patent Applicant/Assignee:
QUALCOMM INCORPORATED, 5775 Morhouse Drive, San Diego, CA 92121-1714, US, US (Residence), US (Nationality)
Inventor(s):
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SINDHUSHAYANA Nagabhushana T, 10615 Dabney Drive #19, San Diego, CA 92126, US
ESTEVES Eduardo A S, 14005H Mango Drive, Del Mar, CA 92014, US
Legal Representative:
WADSWORTH Philip R, Qualcomm Incorporated, 5775 Morehouse Drive, San Diego, CA 92121-1714, US
Patent and Priority Information (Country, Number, Date):
Patent: WO 200070836 A1 20001123 (WO 0070836)
Application: WO 2000US13418 20000515 (PCT/WO US0013418)
Priority Application: US 99311793 19990513
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English

Fulltext Word Count: 11711

Fulltext Availability:
  Detailed Description
  Claims

Detailed Description
... scaling circuit 106 is connected to an input of an LLR multiplier 110, another input of which is connected to an output of the accurate **scaling factor** computation circuit 102. An output of the LLR mutliplier 110 represents an accurate LLR value of the corresponding data sample that is provided to a **turbo decoder** to facilitate **decoding** of the data samples as discussed more fully below.
The data sample SIR circuit 98 computes a data sample SIR based on the C/I...

Claim
... a turbo encoder for encoding a data signal and transmitting said data signal with a pilot signal;
a first rece -%7 er section having a **turbo decoder** and a priori knowledge of said pilot signal for receiving said data signal and said pilot signal and providing an estimate of said channel based...

...SAMPLES
DEMODULATOR ADC SEPARATOR/
DESPREADER
CONTROL SAMPLES
52
ADC SAMPLES
FIG. 4
90 **@o 96
-----------t -----------------------
LLR CIRCUIT
DATA 92 DATA SAMPLE
SIR
SAMPL
ACCURATE **SCALING**
Es
SIRd= 7d **FACTOR** COMPUTATIO
PILOT C/I as,
FROM 2
SAMPLES COMPUTATION
SEPARATOR/
DESPREADER C Es I+ (72 + I+ 7d
GZ2 CHANNEL IV 2,
ESTIMATE SIR X Y...

...186-@) 17c,
174
176 1
PILOT LOWPASS COMPLEX RE ROUGH SCALED
SAMPLES FILTER CONJUGATE LLR VALUE
178
DATA LLR
SA7MPLES GENERATOR
----
r 180 r 182
TURBO DATA OR
DECODER SPEECH
PROCESSING
FIG, 7
190 q @A A
MEsj jOl Xt
70 PILOT 192 1 9
I/Q PN M- CHANNEL+ N/ Ntll LC
DESPREADER...

19/3,K/29 (Item 16 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00750776 **Image available**
STANDARD COMPRESSION WITH DYNAMIC RANGE ENHANCEMENT OF IMAGE REGIONS
COMPRESSION STANDARD AVEC UNE AMELIORATION DE LA PLAGE DYNAMIQUE DE REGIONS D'UNE IMAGE
Patent Applicant/Assignee:
SARNOFF CORPORATION, 201 Washington Road, CN 5300, Princeton, NY 08543-5300, US, US (Residence), US (Nationality)
Inventor(s):
REITMEIER Glenn Arthur, 193 Cinnabar Lane, Yardley, PA 19067, US
TINKER Michael, 35 Highland Drive, Yardley, PA 19067, US
Legal Representative:
NEY Andrew L, Ratner & Prestia, 301 One Westlakes (Berwyn), P.O. Box 980, Valley Forge, PA 19482-0980, US
Patent and Priority Information (Country, Number, Date):
Patent: WO 200064185 A1 20001026 (WO 0064185)
Application: WO 2000US10295 20000417 (PCT/WO US0010295)
Priority Application: US 99292693 19990415
Designated States: CA JP KR SG
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Filing Language: English
Fulltext Word Count: 8304

Fulltext Availability:
Detailed Description

Detailed Description
... 2+(Op
MN)*
TR/[(MAX
M,N)2+(MAX
M,N)]+0.5 (eq. 8)
In the case of rernapping using a tabulated ftinction, the **table** comprises an indexable array of values, where the **index** values are the original range and the values in the **table** are included in the target range. This allows any arbitrary mapping between the two ranges.

Unless, like gamma correction, that mapping is one-way only (i.e., the remapping is not intended to be "umnapped"), then there an inverse table at the **decoder** 550 or inverse **map** and **scale** unit 60 will restore the original infon-nation values.

It should be noted that the terms dynamic range enhancement stream and map region identification stream...

19/3,K/30 (Item 17 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00577941 **Image available**
QUANTIZATION METHOD FOR ITERATIVE DECODER IN COMMUNICATION SYSTEM
PROCEDE DE QUANTIFICATION POUR DECODEUR A ITERATION D'UN SYSTEME DE TELECOMMUNICATIONS
Patent Applicant/Assignee:
SAMSUNG ELECTRONICS CO LTD,
Inventor(s):
KIM Min-Goo,
KIM Beong-Jo;,
LEE Young-Hwan,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200041314 A1 20000713 (WO 0041314)
Application: WO 99KR827 19991228 (PCT/WO KR9900827)

Priority Application: KR 9862715 19981231
Designated States: AU BR CA CN IN JP RU AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 5831

Fulltext Availability:
Claims

Claim
... on an input signal using a maximum a posteriori probability (MAP) algorithm or a soft output Viterbi algorithm (SOVA).

7 A quantization method for a **turbo decoder** in a communication system, comprising the steps ofequally dividing received signal levels into 8 or 16 quantization **scaling factor** intervals using 5 to 7 quantization bits within a range 2' (I is a positive integer) times greater than a transmission signal level range of...

19/3,K/31 (Item 18 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00543950 **Image available**
FORWARD ERROR CORRECTING SYSTEM WITH ENCODERS CONFIGURED IN PARALLEL AND/OR SERIES
SYSTEME DE CORRECTION AVAL DES ERREURS COMPRENANT DES CODEURS CONFIGURES EN PARALLELE ET/OU EN SERIE
Patent Applicant/Assignee:
VOCAL TECHNOLOGIES LTD,
TORRES Juan Alberto,
DEMJANENKO Victor,
HIRZEL Frederic,
Inventor(s):
TORRES Juan Alberto,
DEMJANENKO Victor,
HIRZEL Frederic,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200007323 A1 20000210 (WO 0007323)
Application: WO 99US17369 19990730 (PCT/WO US9917369)
Priority Application: US 9894629 19980730; US 9898394 19980830; US 99133390 19990510
Designated States: JP US AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 65130

Fulltext Availability:
Claims

Claim
... L;
#cIefine UU 19 maxLmn symbol size EXTERN int B;
Odefine BB 5 maximum block delay depth
Ndeflne it 50 maximum lookback length EXTERN double **SCALE** ;
Ndefine 11 680 maximum trellis symbols per frame
EXTERN FILE *spcout;
EXIERN i nt eniblescrambler;
EXTERN int enab I e
r eed
so t omon...

...long crrnr
Iindt [6); extern void free
turbo
memory (void);
EXTERN dOLJh(C SIGMA; extern void init

` DELAY*T should be greater/equat t
o TRELLIS-100KRACK SIZE
n");
SCALE
#undef minimize
#undef maximize
5 - (31) 1) 9 1:38p y:PANDOM-CPP O
Ninctude "test.h"
static doLible **SCALE** ;
static int TIMES;
void
init rarwi(xn (dOUble sigma, int times)
siarid should have been called within the main routine
TIMES times;
SCALE sigma * sqrt (12.0) / sqrt ((double) TIMES);
double
random-value (void)
int i;
doubte tvsull;
result @ 0.0;
for (I = 0; I < TIMES; if+)
result...Alpha exponent for the first root of the generator poiynomiat
Primitive polynomials - see tin & Costello, Appendix A,
and Lee & Messerschmitt, P. 453.
#define BO I
index ->potynomial form conversion **table**
#if (MM == 2) /* Admittedly silly
static int Pp [HM+II = (1, 1, 1 static ST Alpha
to lallocl!N+11;
Netif (MM == 3) /* I + X + X'3
static int Pp (MM+13 = (1, 1, 0, 1 Polynomial-> **index** form conversion
table
Nelif (MM @= 4) /* 1 + x + x'4
Ull 99 1:38p y:[?S.CPP 2 C
static qf **Index** of [aHocNN+I1;
generate GF (2**m) from the irreducible polynomial p (X) in p 101 - -P
CM:
No legal value in **index** form represents zero, so
we need a special value for this purpose lookup **tables** :
index form -> polynomial form atpha-to [I contains j=alpha**i;
#de f i ne AO (UN) polynomial form -> **index** form index
of [j=atpha**il = I
P alpha=2 is the primitive element of GF (2**m)
Generator polynomial 9 (x)
Degree of g...

19/3,K/32 (Item 19 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00505744 **Image available**
REGION-BASED INFORMATION COMPACTION FOR DIGITAL IMAGES
COMPACTAGE D'INFORMATIONS BASEES SUR UNE ZONE POUR IMAGES NUMERIQUES
Patent Applicant/Assignee:
SARNOFF CORPORATION,
Inventor(s):
REITMEIER Glenn A,
TINKER Michael,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9937096 A1 19990722
Application: WO 99US351 19990119 (PCT/WO US9900351)
Priority Application: US 9871296 19980116; US 9871294 19980116; US 9850304 19980330
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE

CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 6431
Fulltext Availability:
Detailed Description

Detailed Description
... OP-MIN)-:.

TR/[(MAX-MIN)2+(MAX-MIN)1+0.51 (eq. 8)
1 6
In the case of remapping using a tabulated function, the **table** comprises
indexable array of values, where the **index** values are the original range and the values in the **table** are included in the target range. This allows any arbitrary mapping between the two ranges. Unless, like gamma correction, that mapping is one-way only (i.e., the remapping is not intended to be "unmapped"), then there an inverse table at the **decoder** 550 or inverse **map** and **scale** unit 60 will restore the original information values.

Although various embodiments which incorporate the teachings of the present invention have been shown and described in...

19/3,K/33 (Item 20 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00282872
RECEIVER FOR A DIRECT SEQUENCE SPREAD SPECTRUM ORTHOGONALLY ENCODED SIGNAL EMPLOYING RAKE PRINCIPLE
RECEPTEUR POUR SIGNAL A CODAGE ORTHOGONAL A SPECTRE ETALE A SEQUENCE DIRECTE, EMPLOYANT LE PRINCIPE DU RATEAU
Patent Applicant/Assignee:
QUALCOMM INCORPORATED,
Inventor(s):
VITERBI Audrey,
VITERBI Andrew,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9501018 A1 19950105
Application: WO 94US6602 19940622 (PCT/WO US9406602)
Priority Application: US 93110 19930624
Designated States: AT BG BR BY CA CN CZ FI HU JP KP KR KZ LV NO PL RO RU SK UA UZ AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 9816

Fulltext Availability:
Detailed Description

Detailed Description
... in coordination with the predetermined
ordering scheme. Selected decision value 146 is input to metric computation mechanism 150 which scales the selected decision value to **scaling factor** 154 which can be used as a **scaling factor** in forming an
individual soft decision data which can subsequently be used in forming **soft decision** transition metrics for maximum likelihood **decoding** techniques.. The index data symbol associated with selected decision value 148 is input to index mapping mechanism 152 which maps the index data symbol into...

...bit length index data symbol maps into 6 soft decision bits). Multiplier 158 multiplies each of the plurality of +/-1 soft decision bits 156 by **scaling factor** 154 to form individual soft decision data 160 for each soft decision bit (e.g., 6 soft

decision

19/3,K/34 (Item 21 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00188821
SOFT DECISION DECODING WITH CHANNEL EQUALIZATION
DECODAGE DE DECISION PROGRAMMABLE A EGALISATION DE CANAL
Patent Applicant/Assignee:
  MOTOROLA INC,
Inventor(s):
  LABEDZ Gerald Paul,
  BORTH David Edward,
  RASKY Phillip David,
Patent and Priority Information (Country, Number, Date):
  Patent: WO 9106165 A1 19910502
  Application: WO 90US5359 19900924 (PCT/WO US9005359)
  Priority Application: US 89177 19891013
Designated States: AT AU BE BR CA CH DE DK ES FI FR GB IT JP KR LU NL NO SE
Publication Language: English
Fulltext Word Count: 2884

Fulltext Availability:
  Detailed Description

Detailed Description
... 1)
for the burst m. If the MLSE hard decisions for a burst m are given by dn,
n = 1 9 . . .1 N then the **soft decision** information passed to the convolutional **decoder** for each of the samples would be
SDn= ...bursts and symbols on a faded channel, making their soft decision values even lower than in the non-scaled case. The length of time the **scaling factor** Om represents can be a variable. The preferred embodiment is for a burst.oriented processing in a Time Division Multiple Access (TDMA) system, and it...

File 347:JAPIO Oct 1976-2003/Jun(Updated 031006)
(c) 2003 JPO & JAPIO
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200369
(c) 2003 Thomson Derwent

Set	Items	Description
S1	750	(SOFT()DECISION? ? OR MAP OR (MAX OR MAXIM?)(3W)(APOSTERIO-R? OR A()POSTERIOR?) OR TURBO)(5N)DECOD?
S2	8271	(LOOKUP? ? OR LOOK???()UP)(3N)TABLE? ? OR LUT OR LUTS
S3	80	N(2W)(ENTRY OR ENTRIES)
S4	17327	(SECOND? OR TWO OR 2ND OR DUAL? OR MULTIPL? OR PLURAL? OR - SEVERAL OR VARIOUS OR DIFFERENT OR SEPARATE OR ASSORT? OR ADD-ITIONAL)(5N)(INDEX??? OR INDICE? ?)
S5	1224	SCALING(3N)FACTOR? ?
S6	38	S2(20N)S3:S4
S7	0	S1 AND S6 AND S5
S8	623	TABLE? ?(20N)S3:S4
S9	1	S1 AND S8 AND S5
S10	1	S1 AND S8 AND SCAL???
S11	292	S2(20N)(INDEX?? OR INDICE? ?)
S12	0	S1 AND S11 AND S5
S13	5310	TABLE? ?(20N)(INDEX?? OR INDICE? ?)
S14	1	S1 AND S13 AND S5
S15	2	S1 AND S13 AND SCAL???
S16	1	S15 NOT S14
S17	20	S1 AND S2:S5
S18	207	S15:S17

18/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

07003064 **Image available**
TURBO DECODER

PUB. NO.: 2001-230681 [JP 2001230681 A]
PUBLISHED: August 24, 2001 (20010824)
INVENTOR(s): SUZUKI HIROSHI
APPLICANT(s): KAWASAKI STEEL CORP
APPL. NO.: 2000-037594 [JP 200037594]
FILED: February 16, 2000 (20000216)
INTL CLASS: H03M-013/29; G06F-011/10; H03M-013/13; H03M-013/27

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **turbo decoder** improved in error correction ability and throughput.

SOLUTION: Concerning a **turbo decoder** 1 for performing **turbo decoding** by inputting **turbo** -encoded data by the unit of a block, the S/N (signal-to-noise ratio) of a signal under processing is estimated by performing the -mean square of soft output data L2 (u*) from a soft output decoder 12 in a -mean square circuit 19, an IER corresponding to that S/N is outputted from a **look - up table** 23, and the levels of input data Ys, Yp1 and Yp2 are controlled by input level control parts 20, 21 and 22.

18/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

07003062 **Image available**
TURBO DECODER

PUB. NO.: 2001-230679 [JP 2001230679 A]
PUBLISHED: August 24, 2001 (20010824)
INVENTOR(s): SUZUKI HIROSHI
APPLICANT(s): KAWASAKI STEEL CORP
APPL. NO.: 2000-036814 [JP 200036814]
FILED: February 15, 2000 (20000215)
INTL CLASS: H03M-013/27; H03M-013/13

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **turbo decoder** , which reduces power consumption.

SOLUTION: Concerning a **turbo decoder** 1 for performing **turbo decoding** by inputting **turbo** -encoded data for the unit of a block, while referring to a **look - up table** 20, the number of times of repetition, corresponding to an estimated signal/noise ratio, is estimated by a root mean circuit 19 and decremented by a counter part 21, so that **turbo decoding** is performed for that number of times of repetition.

18/5/3 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015404578 **Image available**
WPI Acc No: 2003-466719/200344
XRPX Acc No: N03-371286
LUT **(** look **-up** table **) addressing scheme for** turbo decoding **system involves extracting address bits from** index **value and using address bits to address second** table

Patent Assignee: SANTOSA H (SANT-I); YUAN W S (YUAN-I); ZHANG M (ZHAN-I)
Inventor: SANTOSA H; YUAN W S; ZHANG M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030056167	A1	20030320	US 2001905661	A	20010712	200344	B

Priority Applications (No Type Date): US 2001905661 A 20010712
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030056167	A1		19	H03M-013/00	

Abstract (Basic): US 20030056167 A1

NOVELTY - The method entails generating a second **table** having a number of entries based on a first **table** . First and second data fields are then generated and an **index** value is computed. Address bits are extracted from the **index** value. The address bits are used to address the second **table** .

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) a circuit for decoding input data; and

(b) a method in a **decoder** applying the **maximum a - posteriori** probability algorithm for computing a specific function for two argument values.

USE - For **turbo decoding** system of communication systems.

ADVANTAGE - Provides improvements to **turbo decoding** that reduces complexity of **turbo decoder** and reduces **decoder** processing time. Applies to **LUTs** whether **scaled** or not.

DESCRIPTION OF DRAWING(S) - The figure is a block diagram illustrating a complete iteration of a **decoding** operation of a **turbo decoder** .

pp; 19 DwgNo 3/13

Title Terms: UP; TABLE; ADDRESS; SCHEME; TURBO; DECODE; SYSTEM; EXTRACT; ADDRESS; BIT; INDEX; VALUE; ADDRESS; BIT; ADDRESS; SECOND; TABLE
Derwent Class: T01; U14; U21; W01
International Patent Class (Main): H03M-013/00
File Segment: EPI

18/5/4 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015357399 **Image available**
WPI Acc No: 2003-418337/200339
XRPX Acc No: N03-333736

Add-compare-select arithmetic unit for Viterbi decoder, has pair of two's complement adders that perform operations on state metric related to respective bit values

Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: CHOI G S; CHOI G
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030039323	A1	20030227	US 2002189762	A	20020708	200339	B
KR 2003005768	A	20030123	KR 200141215	A	20010710	200339	

Priority Applications (No Type Date): KR 200141215 A 20010710
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030039323	A1		11	H03M-013/03	
KR 2003005768	A			H03M-013/41	

Abstract (Basic): US 20030039323 A1

NOVELTY - A multiplexer (208) selects the smaller output between outputs of 2's complement adders (202,204) which perform operations on state metrics related to bit values 0 and 1 respectively. An absolute value of difference between the outputs of 2's complement adders, is

calculated. A log value corresponding to absolute value is calculated using a **look - up table** (212) and log value is subtracted from multiplexer output.

USE - Add-compare-select (ACS) arithmetic unit for Viterbi **decoder** using **maximum A - posterior (MAP)** algorithm in wireless digital communication system including code division multiple access (CDMA) communication system and wideband CDMA communication system.

ADVANTAGE - Eliminates the normalization, by using the characteristic of modules operation and thereby increasing system through put, reducing latency and realizing efficient ACS and denormalization. Simplifies structure of ACS arithmetic unit, since the need for additional circuits such as comparator, multiplexer and subtractor for normalization operation is eliminated.

DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of the add-compare-select arithmetic unit.

2's complement adders (202,204)
multiplexer (208)
look - up table (212)
pp; 11 DwgNo 4/5

Title Terms: ADD; COMPARE; SELECT; ARITHMETIC; UNIT; VITERBI; DECODE; PAIR; TWO; COMPLEMENTARY; ADDER; PERFORMANCE; OPERATE; STATE; METRIC; RELATED; RESPECTIVE; BIT; VALUE
Derwent Class: U21; W01; W02
International Patent Class (Main): H03M-013/03; H03M-013/41
File Segment: EPI

18/5/5 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015269711 **Image available**
WPI Acc No: 2003-330640/200331
XRPX Acc No: N03-264745

Logarithmic functions computing method in digital communication system, involves generating data field including table values computed based on argument equations and scaling **table values**

Patent Assignee: YUAN W S (YUAN-I)
Inventor: YUAN W S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030014711	A1	20030116	US 2001905568	A	20010712	200331	B

Priority Applications (No Type Date): US 2001905568 A 20010712
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030014711	A1		21	H03M-013/03	

Abstract (Basic): US 20030014711 A1

NOVELTY - A data field including **several table index** values selected from predetermined range of argument values, is generated. The **index** values are **scaled** using a **scaling factor** . Another data field including **table** values computed based on the logarithmic/natural logarithmic equations involving the argument values, is generated. The computed table values are then **scaled** by the **scaling factor** .

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following.

(1) logarithmic functions computing circuit;
(2) data decoding circuit; and
(3) data receiver.

USE - For computing logarithmic/natural logarithmic functions in data decoding circuits (claimed) in digital communication system and wireless communication system using error correction codes.

ADVANTAGE - The **scaling** and decoding operations can be performed with greater efficiency.

DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of the

turbo decoder .
pp; 21 DwgNo 13/13
Title Terms: LOGARITHM; FUNCTION; COMPUTATION; METHOD; DIGITAL; COMMUNICATE ; SYSTEM; GENERATE; DATA; FIELD; TABLE; VALUE; COMPUTATION; BASED; ARGUMENT; EQUATE; **SCALE** ; TABLE; VALUE
Derwent Class: T01; U21; W01
International Patent Class (Main): H03M-013/03
File Segment: EPI

18/5/6 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015265238 **Image available**
WPI Acc No: 2003-326167/200331
Apparatus for calculating llr using non-linear look - up table **in cdma-2000 mobile communication system**
Patent Assignee: HYNIX SEMICONDUCTOR INC (HYNI-N)
Inventor: LEE J H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2002093329	A	20021216	KR 200132041	A	20010608	200331	B

Priority Applications (No Type Date): KR 200132041 A 20010608
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2002093329	A		1	H04B-007/216	

Abstract (Basic): KR 2002093329 A
NOVELTY - An apparatus for calculating an LLR(Log Likelihood Ratio) using a non-linear **look - up table** in a CDMA(Code Division Multiple Access)-2000 mobile communication system is provided to improve an error correction performance by calculating the LLR using the non-linear **look - up table** in a **turbo decoder .**
DETAILED DESCRIPTION - A demodulator(500) demodulates received data. A **MAP** (**Maximum A Posteriori**) **decoder** (600) corrects the signal demodulated in the demodulator(500). The **MAP decoder** (600) has a branch matrix calculator for calculating a branch matrix from the signal demodulated in the demodulator(500), and a backward/forward state matrix calculator for calculating a backward/forward state matrix from the demodulated signal through the branch matrix calculator. The **MAP decoder** (600) has an LLR calculator for comparing the branch matrix calculating value and the backward/forward state matrix calculating value with a non-linear **look - up table** , and calculating an LLR.
pp; 1 DwgNo 1/10
Title Terms: APPARATUS; CALCULATE; NON; LINEAR; UP; TABLE; CDMA; MOBILE; COMMUNICATE; SYSTEM
Derwent Class: W02
International Patent Class (Main): H04B-007/216
File Segment: EPI

18/5/7 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015214808 **Image available**
WPI Acc No: 2003-275345/200327
XRPX Acc No: N03-218593
Bit-error rate estimation method used in wireless receiver, involves processing received wireless signal to generate Yamamoto-Itoh metric, and estimating bit error rate of received signal as function of YI metric
Patent Assignee: MONOGIOUDIS P (MONO-I); REGE K M (REGE-I)
Inventor: MONOGIOUDIS P; REGE K M
Number of Countries: 001 Number of Patents: 001

Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 20020172302 A1 20021121 US 2001808376 A 20010314 200327 B

Priority Applications (No Type Date): US 2001808376 A 20010314
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20020172302 A1 16 H03D-001/00

Abstract (Basic): US 20020172302 A1
NOVELTY - The received wireless signal is processed to provide a Yamamoto-Itoh (YI) metric value. An initial bit-error-rate (BER) estimate value is selected from a **look - up table** , as a function of the Yamamoto-Itoh (YI) metric value, and modified with a retrieved compensation factor value, to provide a BER estimate for the received signal. The compensation factor value is determined as a function of the YI metric value.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) BER estimation apparatus; and

(2) wireless receiver.

USE - For estimating BER used in wireless receiver (claimed) of universal mobile telecommunication system (UMTS).

ADVANTAGE - The BER estimate of received signal is directly determined using YI metric values, without using iterative **decoding** methods based on **maximum Aposteriori** probability (**MAP**) **decoders** .

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the wireless end point.

pp; 16 DwgNo 1/9
Title Terms: BIT; ERROR; RATE; ESTIMATE; METHOD; WIRELESS; RECEIVE; PROCESS ; RECEIVE; WIRELESS; SIGNAL; GENERATE; METRIC; ESTIMATE; BIT; ERROR; RATE ; RECEIVE; SIGNAL; FUNCTION; METRIC
Derwent Class: U21; W01; W02
International Patent Class (Main): H03D-001/00
International Patent Class (Additional): H04L-027/06
File Segment: EPI

18/5/8 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014900135 **Image available**
WPI Acc No: 2002-720841/200278
Turbo decoder **in mobile communication base station**
Patent Assignee: HYNIX SEMICONDUCTOR INC (HYNI-N)
Inventor: LEE J H
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
KR 2002041567 A 20020603 KR 200071224 A 20001128 200278 B

Priority Applications (No Type Date): KR 200071224 A 20001128
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
KR 2002041567 A 1 H03M-013/39

Abstract (Basic): KR 2002041567 A
NOVELTY - A **turbo decoder** in a mobile communication base station is provided to reduce hardware complexity in designing a chip set and variably use values of a **look up table** using a power control bit.

DETAILED DESCRIPTION - A selector(100) receives a power control bit among a transmission signal inputted through a demodulator. The selector(100) confirms the number of '0' and '1' in a power control bit and determines a Sel value according the number of confirmed '0' and '1'. A **look up table** (200) obtains and stores a deviation of a

channel noise obtained in an initial synchronization of a mobile communication base station. A multiplexer(300) multiplies the Sel value from the selector(100) by an L value from the **look up table** (200) and outputs a channel noise N. A BM calculator(400) calculates a branch matrix using xk and yk from a demodulator an N from the multiplexer(300).

pp; 1 DwgNo 1/10

Title Terms: TURBO; DECODE; MOBILE; COMMUNICATE; BASE; STATION
Derwent Class: U21
International Patent Class (Main): H03M-013/39
File Segment: EPI

18/5/9 (Item 7 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014870361 **Image available**
WPI Acc No: 2002-691067/200274
XRPX Acc No: N02-545193

Turbo decoder **for wireless communication system e.g. international mobile telecommunication-2000, has** lookup table **to apply base-2 logarithm on shifted decimal part added to maximum integral value to obtain final value**

Patent Assignee: ELECTRONICS & TELECOM RES INST (ELTE-N); KOREA ELECTRONICS & TELECOM RES INST (KOEL-N); CHO H (CHOH-I); JEON I (JEON-I); KIM H (KIMH-I); KIM K (KIMK-I); YANG W (YANG-I)
Inventor: CHO H J; JUN I S; KIM G S; KIM H; YANG U S; JEON I S; YANG W S; CHO H; JEON I; KIM K; YANG W
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020116680	A1	20020822	US 2001966201	A	20010926	200274	B
KR 2002054203	A	20020706	KR 200083169	A	20001227	200303	
KR 365724	B	20021231	KR 200083169	A	20001227	200337	

Priority Applications (No Type Date): KR 200083169 A 20001227
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020116680	A1		14	H03M-013/03	
KR 2002054203	A			H03M-013/37	
KR 365724	B			H03M-013/37	Previous Publ. patent KR 2002054203

Abstract (Basic): US 20020116680 A1

NOVELTY - A **lookup table** (43) calculates the sum of exponential terms of base-2 function in decimal parts of input state metrics (A,B). A **lookup table** (48) applies base-2 logarithm on the decimal part added to maximum value of metric integral part, after shifting. An adder (49) adds the maximum integral value with the table output to obtain a final base-2 function.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) **Turbo** codes **decoding** method for **turbo decoder** ; and

(2) Computer-readable medium storing **turbo** codes **decoding** program.

USE - For **decoding turbo** codes which are used as error correction codes for high speed data transmission in wireless communication system such as international mobile telecommunication (IMT)-2000 using base-2 binary LogMAP algorithm.

ADVANTAGE - The use of base-2 binary LogMAP algorithm decreases the computational burden needed to calculate the value of forward and backward state metrics and reduces the hardware required for **decoding turbo** codes, enhances the speed of **decoding** the codes and increases precision of decoding table.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of base-2 function calculator.

Lookup tables (43,48)

Adder (49)

Input state metrics (A,B)
pp; 14 DwgNo 4/6
Title Terms: TURBO; DECODE; WIRELESS; COMMUNICATE; SYSTEM; INTERNATIONAL; MOBILE; TELECOMMUNICATION; TABLE; APPLY; BASE; LOGARITHM; SHIFT; DECIMAL; PART; ADD; MAXIMUM; INTEGRAL; VALUE; OBTAIN; FINAL; VALUE
Derwent Class: T01; U21
International Patent Class (Main): H03M-013/03; H03M-013/37
File Segment: EPI

18/5/10 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014669129 **Image available**
WPI Acc No: 2002-489833/200252
XRPX Acc No: N02-387253
Soft decision **maximum likelihood encoder and** decoder **for codes that operate on symbols rather than on bits and that include forward error correcting code**
Patent Assignee: ITRAN COMMUNICATIONS LTD (ITRA-N)
Inventor: BARKAN G; RAPHAELI D
Number of Countries: 094 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200231983	A2	20020418	WO 2001IL920	A	20011003	200252	B
AU 200195860	A	20020422	AU 200195860	A	20011003	200254	

Priority Applications (No Type Date): US 2000686237 A 20001011
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
WO 200231983 A2 E 53 H03M-013/00
Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW
AU 200195860 A H03M-013/00 Based on patent WO 200231983

Abstract (Basic): WO 200231983 A2
NOVELTY - A **soft decision decoder** (44) includes a correlation-to-log probability ratio module (60) receiving correlated values (40) and shift indexes (42) and forming a maximum likelihood ratio value (78) for input to a compressor (62). The compressed value is input to a memory (64), is decompressed by an expander (66) using a shift index provided by a module (68) as a **lookup table** and is output as a log probability to module (68). An erasure generator module (74) generates and outputs an erasure pattern for each erasure combination and a decode state machine (72) generates the decoded data for output.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for a method of **soft decision decoding ,** for a method of generating a soft decision error correcting code and for communication apparatus.

USE - **Soft decision decoding** in code shift keying.

DESCRIPTION OF DRAWING(S) - The drawing shows a decoder
Decoder (44)
Probability ratio module (60)
Compressor (62)
Expander (66)
Erasure generator module (74)
Decode state machine (72)
pp; 53 DwgNo 4/5
Title Terms: SOFT; DECIDE; MAXIMUM; ENCODE; DECODE; CODE; OPERATE; SYMBOL; BIT; FORWARD; ERROR; CORRECT; CODE
Derwent Class: U21; W02
International Patent Class (Main): H03M-013/00
File Segment: EPI

18/5/11 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014633865 **Image available**
WPI Acc No: 2002-454569/200248
XRPX Acc No: N02-358507
Improved decoding **of** turbo **codes using data scaling of convolutionally coded input data to provide near ideal** turbo decoding **in coded communication system**
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: DINC A; FONTAINE F M; ABDULKADIR D
Number of Countries: 097 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200231964	A1	20020418	WO 2001US42450	A	20011002	200248	B
US 6393076	B1	20020521	US 2000686575	A	20001011	200248	
AU 200211845	A	20020422	AU 200211845	A	20011002	200254	

Priority Applications (No Type Date): US 2000686575 A 20001011
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
WO 200231964 A1 E 21 H03D-001/00
Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW
US 6393076 B1 H03D-001/00
AU 200211845 A H03D-001/00 Based on patent WO 200231964

Abstract (Basic): WO 200231964 A1
NOVELTY - A portion of input data is loaded into a buffer, 102, a mean of the data in this portion is calculated, 104, the root-mean-square value of this portion is calculated, 106 and a **scaling factor** is derived from the root-mean-square value, 108. The portion of input data is then scaled by the derived **scaling factor**, 110 and the scaled data are sent to a **turbo decoder** for **decoding**. The process is repeated until all input data are decoded.
USE - Decoding of convolutionally coded data in communication system decoder.
ADVANTAGE - No reliance on channel estimation as base for scaling.
DESCRIPTION OF DRAWING(S) - The drawing shows the decoding method.
pp; 21 DwgNo 10/10
Title Terms: IMPROVE; DECODE; TURBO; CODE; DATA; SCALE; CODE; INPUT; DATA; IDEAL; TURBO; DECODE; CODE; COMMUNICATE; SYSTEM
Derwent Class: U21; W01
International Patent Class (Main): H03D-001/00
International Patent Class (Additional): H04L-027/06
File Segment: EPI

18/5/12 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014241360 **Image available**
WPI Acc No: 2002-062060/200208
Related WPI Acc No: 2002-381287
XRPX Acc No: N02-046090
Iteration terminating using quality index criteria of turbo codes for e.g. direct sequence code division multiple access communications system using two recursion processors
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: TEICHER H; XU S J

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Number of Countries: 094  Number of Patents: 003
Patent Family:
Patent No     Kind  Date     Applicat No    Kind  Date     Week
WO 200182486   A1  20011101  WO 2001US11544  A   20010410  200208  B
AU 200153295   A   20011107  AU 200153295    A   20010410  200219
EP 1314254     A1  20030528  EP 2001926783   A   20010410  200336
                             WO 2001US11544  A   20010410

Priority Applications (No Type Date): US 2000553646 A 20000420
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
WO 200182486  A1 E  26 H03M-013/00
   Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA
   CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP
   KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT
   RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
   Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR
   IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW
AU 200153295  A        H03M-013/00   Based on patent WO 200182486
EP 1314254    A1 E     H03M-013/00   Based on patent WO 200182486
   Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT
   LI LT LU LV MC MK NL PT RO SE SI TR
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Abstract (Basic): WO 200182486 A1

NOVELTY - A decoder dynamically terminates iteration calculations in the decoding of a received convolutionally coded signal using quality index criteria.

DETAILED DESCRIPTION - The **turbo decoder** has two recursion processors connected in an iterative loop, with an additional recursion processor coupled in parallel at the inputs of the recursion processors. All of the recursion processors perform concurrent iterative calculations on the signal. The a **additional** recursion processor calculates a quality **index** of the signal for each iteration. A controller terminates the iterations when the measure of the quality index criteria exceeds a set level.

USE - for decoding convolutional codes used in e.g. direct sequence code division multiple access (DS-DCMA) communications system.

ADVANTAGE - Can determine the appropriate stopping point for the iterations in a reliable manner.

DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram of the **turbo decoder** .

pp; 26 DwgNo 4/11

Title Terms: ITERATIVE; TERMINATE; QUALITY; INDEX; CRITERIA; TURBO; CODE; DIRECT; SEQUENCE; CODE; DIVIDE; MULTIPLE; ACCESS; COMMUNICATE; SYSTEM; TWO; PROCESSOR
Derwent Class: U21; W01
International Patent Class (Main): H03M-013/00
International Patent Class (Additional): H04L-027/06
File Segment: EPI

18/5/13 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014211952 **Image available**
WPI Acc No: 2002-032649/200204
Method for decoding turbo **code and** decoder
Patent Assignee: LG ELECTRONICS INC (GLDS)
Inventor: REDEUKOPEU V; SAL M

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Number of Countries: 001  Number of Patents: 001
Patent Family:
Patent No     Kind  Date     Applicat No    Kind  Date     Week
KR 2001069198  A   20010723  KR 200026737    A   20000518  200204  B

Priority Applications (No Type Date): US 2000480004 A 20000110
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
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KR 2001069198 A   1 H03M-013/03

Abstract (Basic): KR 2001069198 A

NOVELTY - A method for **decoding** a **turbo** code and a **decoder** are provided to supply a method for decoding the digital data including the high correct function and to improve the quality of the turbo code and to supply a transmitting channel with the low signal to noise ratio.

DETAILED DESCRIPTION - In the method for **decoding** the **turbo** code and the **decoder** , a few stages are included. In the first stage, the data elements are decoded, which are received by more than two decoding progresses. In the second stage, at least more than two decoding progresses are repeated. The first and second stages are composed of a stage for estimating the parameter of the received data elements, a stage for calculating the **scaling factor** and a stage for formalizing the medium decoded data elements. In the third stage, the decoding progress is finished in advance before the final repetition of two decoding progresses on basis of the output of two decoding progresses. In the fourth stage, the decoded data elements are output.

pp; 1 DwgNo 1/10

Title Terms: METHOD; DECODE; TURBO; CODE; DECODE
Derwent Class: U21
International Patent Class (Main): H03M-013/03
File Segment: EPI

18/5/14 (Item 12 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014139322 **Image available**
WPI Acc No: 2001-623533/200172

Repeated decoding preset apparatus of decoder and method of the same

Patent Assignee: KOREA TELECOM (KOTE-N)
Inventor: JANG J S; JUNG B H; LEE H S; LEE M H; LEE M S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2001048292	A	20010615	KR 9952950	A	19991126	200172	B

Priority Applications (No Type Date): KR 9952950 A 19991126
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2001048292	A		1	H04B-015/00	

Abstract (Basic): KR 2001048292 A

NOVELTY - A repeated decoding preset apparatus of a decoder and a method of the same are provided to preset the number of repeated decoding operations based on an input noise distribution estimation method and an adaptive stop reference structure for thereby decreasing a computation amount and delay due to the repeated number of decoding.

DETAILED DESCRIPTION - A repeated decoding number preset apparatus(310) estimates an input noise distribution based on an output noise distribution of a **MAP decoder1** and adaptively presents a repeated decoding number. A repeated decoding number controller(320) controls a repeated decoding number based on a set value from the repeated decoding number preset apparatus. A decoder(330) performs a decoding operation based on a control of the repeated decoding number controller. The repeated decoding number preset apparatus(310) includes an estimation unit(314) for obtaining an output noise distribution using an average value of an LLR value measured in an output terminal of the **MAP decoder1** , a repeated **decoding** number preset block(313) for obtaining a repeated decoding number which satisfies the performance required by the repeated decoding number **look - up table** (311) using the signal-to-noise ratio and setting the repeated decoding number from the second repeated decoding operation, and an input noise distribution **look - up table** (312) for storing the input noise

distribution.
pp; 1 DwgNo 1/10
Title Terms: REPEAT; DECODE; PRESET; APPARATUS; DECODE; METHOD
Derwent Class: W02
International Patent Class (Main): H04B-015/00
File Segment: EPI

18/5/15 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014105569 **Image available**
WPI Acc No: 2001-589783/200166
XRPX Acc No: N01-439335

Recursive convolutional symbols decoding method in wireless communication system, involves linearly combining multiple bits defining current state of backward recursion process and hypothesized information bit

Patent Assignee: MOTOROLA INC (MOTI)
Inventor: BROWN T; WANG M M
Number of Countries: 022 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200161891	A1	20010823	WO 2001US3355	A	20010201	200166	B
KR 2001113792	A	20011228	KR 2001712997	A	20011012	200240	
US 6580769	B1	20030617	US 2000503791	A	20000214	200341	
JP 2003523691	W	20030805	JP 2001560567	A	20010201	200353	
			WO 2001US3355	A	20010201		

Priority Applications (No Type Date): US 2000503791 A 20000214
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200161891	A1	E	17	H04Q-001/00	

Designated States (National): JP KR
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2001113792	A			H03M-013/23	
US 6580769	B1			H04Q-001/00	
JP 2003523691	W		16	H03M-013/39	Based on patent WO 200161891

Abstract (Basic): WO 200161891 A1
NOVELTY - A forward recursion process is performed on received recursive convolutionally generated symbols. A backward recursion process is then performed to the symbols. The next state for backward recursion process is determined by linearly combining multiple bits defining the current state of backward recursion process and a hypothesized information bit (212un).
USE - For recursive convolutional symbol **decoding** in **soft decision** output **decoders** such as **maximum a posteriori** (**MAP**) **decoders** in code division multiple access (CDMA) based wireless communication systems for multimedia communication.
ADVANTAGE - The linear combination for next state backward recursion process determination is performed using any suitable hardware or software. An efficient recursive convolutional decoder is obtained without need for **look - up table** .
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of backward state determination.
Hypothesized information bit (212un)
pp; 17 DwgNo 2/5

Title Terms: RECURSIVE; CONVOLUTE; SYMBOL; DECODE; METHOD; WIRELESS; COMMUNICATE; SYSTEM; LINEAR; COMBINATION; MULTIPLE; BIT; DEFINE; CURRENT; STATE; BACKWARD; PROCESS; INFORMATION; BIT
Derwent Class: U21; W01; W02
International Patent Class (Main): H03M-013/23; H03M-013/39; H04Q-001/00
International Patent Class (Additional): G06F-017/10
File Segment: EPI

18/5/16 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014097768 **Image available**
WPI Acc No: 2001-581982/200165
XRPX Acc No: N01-433599
Turbo decoder **estimates the** decoding **operations using a reduced power supply**
Patent Assignee: KAWASAKI STEEL CORP (KAWI); KONDO H (KOND-I); SUZUKI H (SUZU-I)
Inventor: KONDO H; SUZUKI H
Number of Countries: 028 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200161867	A1	20010823	WO 2001JP1030	A	20010214	200165	B
JP 2001230677	A	20010824	JP 200037593	A	20000216	200165	
JP 2001230679	A	20010824	JP 200036814	A	20000215	200165	
JP 2001230681	A	20010824	JP 200037594	A	20000216	200165	
EP 1170870	A1	20020109	EP 2001904429	A	20010214	200205	
			WO 2001JP1030	A	20010214		
US 20020168033	A1	20021114	WO 2001JP1030	A	20010214	200277	
			US 2001958285	A	20011010		

Priority Applications (No Type Date): JP 200037594 A 20000216; JP 200036814 A 20000215; JP 200037593 A 20000216
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200161867	A1	J	30	H03M-013/09	

Designated States (National): US
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001230677	A		8	H03M-013/09	
JP 2001230679	A		6	H03M-013/27	
JP 2001230681	A		6	H03M-013/29	
EP 1170870	A1	E		H03M-013/09	Based on patent WO 200161867

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020168033	A1			H04L-027/06	

Abstract (Basic): WO 200161867 A1
NOVELTY - A **turbo decoder** (1) receiving **turbo decoded** data in units of a block and performing **turbo decoding** and operating with reduced power consumption mode. The **turbo decoder** (1) estimates the number of repetition corresponding to the signal-to-noise ratio estimated by a square mean circuit (20) with reference to a **lookup table** (21), decrements it at a counter section (22) and repeats **turbo decoding** the estimated number of times.
USE - **Turbo decoder** estimates the **decoding** operations using a reduced power supply
DESCRIPTION OF DRAWING(S) - **Turbo decoder** (1)
Square mean circuit (20)
Lookup table (21)
Counter section (22)
pp; 30 DwgNo 1/4
Title Terms: TURBO; DECODE; ESTIMATE; DECODE; OPERATE; REDUCE; POWER; SUPPLY
Derwent Class: U21; W01
International Patent Class (Main): H03M-013/09; H03M-013/27; H03M-013/29; H04L-027/06
International Patent Class (Additional): G06F-011/10; H03M-013/13; H03M-013/23; H03M-013/39; H03M-013/41; H03M-013/45; H04L-001/22
File Segment: EPI

18/5/17 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013707001 **Image available**
WPI Acc No: 2001-191225/200119
XRPX Acc No: N01-135937

Receiver system for CDMA communication system, computes LLR ratio as function of channel estimate based on received pilot signal, which is scaled by specified LLR ratio scaling factor **to provide accurate LLR value**

Patent Assignee: QUALCOMM INC (QUAL-N); ESTEVES E A S (ESTE-I); LING F (LING-I); SINDHUSHAYANA N T (SIND-I)
Inventor: ESTEVES E A S; LING F; SINDHUSHAYANA N T
Number of Countries: 093 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200070836	A1	20001123	WO 2000US13418	A	20000515	200119	B
AU 200048523	A	20001205	AU 200048523	A	20000515	200119	
EP 1177662	A1	20020206	EP 2000930760	A	20000515	200218	
			WO 2000US13418	A	20000515		
US 6377607	B1	20020423	US 99311793	A	19990513	200232	
US 20020097785	A1	20020725	US 99311793	A	19990513	200254	
			US 200250338	A	20020115		
KR 2002089127	A	20021129	KR 2001714466	A	20011113	200322	
CN 1413403	A	20030423	CN 2000812594	A	20000515	200347	
JP 2003520463	W	20030702	JP 2000619171	A	20000515	200352	
			WO 2000US13418	A	20000515		
BR 200010475	A	20030715	BR 200010475	A	20000515	200365	
			WO 2000US13418	A	20000515		

Priority Applications (No Type Date): US 99311793 A 19990513; US 200250338 A 20020115
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200070836	A1	E	48	H04L-025/02	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
AU 200048523	A				Based on patent WO 200070836
EP 1177662	A1	E		H04L-025/02	Based on patent WO 200070836

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6377607	B1			H04B-001/69	
US 20020097785	A1			H04K-001/00	Cont of application US 99311793
KR 2002089127	A			H04B-001/69	
CN 1413403	A			H04L-025/02	
JP 2003520463	W		52	H04B-001/707	Based on patent WO 200070836
BR 200010475	A			H04L-025/02	Based on patent WO 200070836

Abstract (Basic): WO 200070836 A1

NOVELTY - C/I ratio computing circuit (92) receives composite signal and outputs pilot and data signal to LLR circuit (96) that computes LLR as function of channel estimate based on pilot signal. Scaling circuit (106) scales computed LLR ratio by specified LLR ratio **scaling factor** and provides accurate LLR values. **Turbo decoder decodes** received composite signal, based on accurate LLR value and data signal.

DETAILED DESCRIPTION - The C/I circuit computes two signal-to-interference ratios based on data and pilot samples in data and pilot signals.

USE - For use with wireless CDMA cellular communication system e.g. mobile telephones.

ADVANTAGE - Provides optimal log-likelihood value, which may greatly enhance the performance of communication system employing **turbo decoding** and encoding. By the provision of unique carrier signal-to-interferences ratio computing circuit, more accurate estimation of noise and interference component of received signal is

realized.
DESCRIPTION OF DRAWING(S) - The figure shows block diagram of telecommunication/receiver system.
Circuits (92,96,106)
pp; 48 DwgNo 5/9
Title Terms: RECEIVE; SYSTEM; CDMA; COMMUNICATE; SYSTEM; COMPUTATION; RATIO ; FUNCTION; CHANNEL; ESTIMATE; BASED; RECEIVE; PILOT; SIGNAL; SCALE; SPECIFIED; RATIO; SCALE; FACTOR; ACCURACY; VALUE
Derwent Class: W01; W02
International Patent Class (Main): H04B-001/69; H04B-001/707; H04K-001/00; H04L-025/02
International Patent Class (Additional): H03M-013/25; H03M-013/29
File Segment: EPI

18/5/18 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013557005 **Image available**
WPI Acc No: 2001-041212/200105
XRPX Acc No: N01-030708
Adaptive maximum aposteriori **probability channel** decoding **apparatus in communication system, has** maximum aposteriori **probability channel** decoder **which selectively operates in two modes according to preset equations**
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: KIM B; KIM M; KIM B J; KIM M G
Number of Countries: 026 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200074399	A1	20001207	WO 2000KR554	A	20000529	200105	B
AU 200051108	A	20001218	AU 200051108	A	20000529	200118	
EP 1101369	A1	20010523	EP 2000935678	A	20000529	200130	
			WO 2000KR554	A	20000529		
KR 2000075096	A	20001215	KR 9919476	A	19990528	200131	
CN 1310924	A	20010829	CN 2000800950	A	20000529	200176	
KR 300306	B	20010926	KR 9919476	A	19990528	200233	
JP 2003501904	W	20030114	WO 2000KR554	A	20000529	200306	
			JP 2001500571	A	20000529		
AU 759490	B	20030417	AU 200051108	A	20000529	200333	
JP 3428977	B2	20030722	WO 2000KR554	A	20000529	200350	
			JP 2001500571	A	20000529		

Priority Applications (No Type Date): KR 9919476 A 19990528
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200074399	A1	E	26	H04Q-007/20	
Designated States (National): AU BR CA CN IN JP					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
AU 200051108	A				Based on patent WO 200074399
EP 1101369	A1	E		H04Q-007/20	Based on patent WO 200074399
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
KR 2000075096	A			H04Q-007/20	
CN 1310924	A			H04Q-007/20	
KR 300306	B			H04Q-007/20	Previous Publ. patent KR 2000075096
JP 2003501904	W		32	H04L-001/00	Based on patent WO 200074399
AU 759490	B			H04Q-007/20	Previous Publ. patent AU 200051108
					Based on patent WO 200074399
JP 3428977	B2		10	H04L-001/00	Previous Publ. patent JP 200301904
					Based on patent WO 200074399

Abstract (Basic): WO 200074399 A1
NOVELTY - A channel estimator (420) calculates the channel noise power and sealing factor. A controller (430) determines the operation mode according to the channel noise power and **scaling factor** . A

maximum aposteriori probability (**MAP**) channel **decoder** (440) has an operator for selectively operating in static channel mode and time varying mode, according to specific equations.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for adaptive **MAP** channel **decoding** method.

USE - For data transmission in radio telecommunication system.

ADVANTAGE - Enables decoding stably regardless of noise power in channel environment of mobile communication system.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of **MAP** recursive **decoding** apparatus.

Channel estimator (420)
Controller (430)
MAP channel **decoder** (440)
pp; 26 DwgNo 4/6

Title Terms: ADAPT; MAXIMUM; PROBABILITY; CHANNEL; DECODE; APPARATUS; COMMUNICATE; SYSTEM; MAXIMUM; PROBABILITY; CHANNEL; DECODE; SELECT; OPERATE; TWO; MODE; ACCORD; PRESET; EQUATE
Derwent Class: W01; W02
International Patent Class (Main): H04L-001/00; H04Q-007/20
International Patent Class (Additional): G06F-011/10; H03M-013/35; H03M-013/41
File Segment: EPI

18/5/19 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013466577 **Image available**
WPI Acc No: 2000-638520/200061
XRPX Acc No: N00-473604

Address generator for turbo interleaver/deinterleaver, has first counter for counting clock pulses, second counter receiving carry and generating position count, together with controller, bit reverser, operating device and buffer

Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: KIM B; KIM M; LEE Y; KIM B J; KIM M G; LEE Y H
Number of Countries: 028 Number of Patents: 011
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200060751	A1	20001012	WO 2000KR301	A	20000403	200061	B
AU 200036817	A	20001023	AU 200036817	A	20000403	200107	
BR 200005569	A	20010306	BR 20005569	A	20000403	200118	
			WO 2000KR301	A	20000403		
EP 1092270	A1	20010418	EP 2000915576	A	20000403	200123	
			WO 2000KR301	A	20000403		
KR 2000066035	A	20001115	KR 9912859	A	19990402	200127	
CN 1297616	A	20010530	CN 2000800461	A	20000403	200156	
AU 746913	B	20020502	AU 200036817	A	20000403	200238	
RU 2186460	C1	20020727	RU 2000130216	A	20000403	200262	
			WO 2000KR301	A	20000403		
JP 2002541711	W	20021203	JP 2000610134	A	20000403	200309	
			WO 2000KR301	A	20000403		
US 6590951	B1	20030708	US 2000541774	A	20000403	200353	
JP 3447270	B2	20030916	JP 2000610134	A	20000403	200361	
			WO 2000KR301	A	20000403		

Priority Applications (No Type Date): KR 9912859 A 19990402
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200060751	A1	E	41	H03M-013/27	

Designated States (National): AU BR CA CN IN JP RU
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
AU 200036817	A			H03M-013/27	Based on patent WO 200060751
BR 200005569	A			H03M-013/27	Based on patent WO 200060751
EP 1092270	A1	E		H03M-001/00	Based on patent WO 200060751

Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI

LU MC NL PT SE

KR 2000066035	A		H03M-013/00	
CN 1297616	A		H03M-013/27	
AU 746913	B		H03M-013/27	Previous Publ. patent AU 200036817 Based on patent WO 200060751
RU 2186460	C1		H03M-013/27	Based on patent WO 200060751
JP 2002541711	W	51	H03M-013/27	Based on patent WO 200060751
US 6590951	B1		H04L-023/00	
JP 3447270	B2	24	H03M-013/27	Previous Publ. patent JP 200241711 Based on patent WO 200060751

Abstract (Basic): WO 200060751 A1

NOVELTY - The address generator has a first counter for counting clock pulses, a second counter receiving a carry from the first counter and generating a position count. There is also a controller, a bit reverser, an operating device and a buffer.

DETAILED DESCRIPTION - The address generator comprises a first counter for counting clock pulses and generating a group count. This consists of k bits indicating one of the 2k groups at each clock pulse. The counter generates a carry after counting 2k clock pulses. A second counter receives the carry from the first counter, and counts the carry, to generate a position count consisting of n bits indicating one of the 2n position addresses. A controller stores unavailable group count values representing the unavailable groups. Partially unavailable group count values representing the groups having both available and unavailable position addresses, are also stored. Unavailable position count values represent the unavailable position addresses. The controller also regulates the first and second counters not to output the group count and the position count, if the group count is one of the unavailable count values, or the group count is one of the partially available group count values and the position count is one of the unavailable position count values. There is also a bit reverser for receiving and reversing the k bits from the first counter. An operating device receives the group count and the position count, and determines an initial seed value corresponding to the received group count, for determining the result bits, according to a predetermined mathematical relationship. A buffer is provided for storing an available address formed from the reverse bits from the reverser, and the result bits from the operating device. INDEPENDENT CLAIMS are included for a method of generating available addresses.

USE - For generating available addresses, which are fewer than 2k+n complete addresses, and in which the complete addresses are divided into 2k groups each having 2n position addresses, without generating unavailable complete addresses. Especially in radio communications systems such as satellite system and digital cellular system.

ADVANTAGE - Improves the distance property of the codewords in a turbo encoder. Maintains the clock timing in a **turbo decoder** to be constant. Reduces the hardware complexity in implementing a **turbo decoder** .

DESCRIPTION OF DRAWING(S) - The figure shows a schematic block diagram illustrating the turbo interleaving address generator.

Adder (120)

Look up table (130)

Bit reverser (140)

Multiplication and modulo (150)

Controller (200)

Counter (210)

pp; 41 DwgNo 3/7

Title Terms: ADDRESS; GENERATOR; TURBO; INTERLEAVED; FIRST; COUNTER; COUNT; CLOCK; PULSE; SECOND; COUNTER; RECEIVE; CARRY; GENERATE; POSITION; COUNT; CONTROL; BIT; REVERSE; OPERATE; DEVICE; BUFFER

Derwent Class: U21

International Patent Class (Main): H03M-001/00; H03M-013/00; H03M-013/27; H04L-023/00

International Patent Class (Additional): G06F-011/10; H03M-013/29

File Segment: EPI

18/5/20 (Item 18 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007625086 **Image available**
WPI Acc No: 1988-259018/198837
XRPX Acc No: N88-196608

Combined encoding and modulation of indexed digital signals - produces code symbol representative of indexing vector having same dimension as corresp. one of ordered sub-spaces

Patent Assignee: SPACE SYSTEMS/LORAL INC (SPAC-N); FORD AEROSPACE & COMMUNIC CORP (FORD)
Inventor: TANNER R M
Number of Countries: 006 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 282298	A	19880914	EP 88302080	A	19880310	198837	B
JP 63237646	A	19881004	JP 8856458	A	19880311	198845	
US 4882733	A	19891121	US 8725768	A	19870313	199005	
CA 1308197	C	19920929	CA 560058	A	19880229	199245	

Priority Applications (No Type Date): US 8725768 A 19870313
Cited Patents: 6.Jnl.Ref; A3...9133; EP 122805; No-SR.Pub; US 4077021
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 282298	A	E	18		
Designated States (Regional): DE FR GB					
US 4882733	A		18		
CA 1308197	C			H03M-013/00	

Abstract (Basic): EP 282298 A

The combined coding and modulation method involves creating signal sets from available amplitude and phase modulations by the indexing of ordered subspaces which need not be binary. Each indexing vector is associated with a Euclidean distance in modulation space so that any **two** modulations whose **indexing** vectors differ only by a distance vector contained in a subspace and any preceding (higher significant) subspaces are separated in the modulation space by the Euclidean distance.

For the particular instance of 8SK modulation on a white Gaussian noise channel, the least significant bit is encoded (206) in a length-73 perfect-difference-set code with 45 information bits and min. distance 10, shortened by one bit. For the centre bit the code is a (72,63,4) shortened Hamming code (204); the most significant bit (202) is uncoded.

USE/ADVANTAGE - Esp. for TDMA operation in e.g. an FDMA satellite transponder channel, signal sets are widely sepd. and unlikely to be confused by effects of channel noise. **Soft decision decoding** develops accurate estimates of information from received signal in computationally efficient manner.

Title Terms: COMBINATION; ENCODE; MODULATE; INDEX; DIGITAL; SIGNAL; PRODUCE ; CODE; SYMBOL; REPRESENT; INDEX; VECTOR; DIMENSION; CORRESPOND; ONE; ORDER; SUB; SPACE
Index Terms/Additional Words: TDMA; FDMA; SATELLITE; TRANSPONDER
Derwent Class: U21; W01; W02
International Patent Class (Additional): G06F-011/10; H03M-013/12; H04L-027/18
File Segment: EPI

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File 275:Gale Group Computer DB(TM) 1983-2003/Oct 27
         (c) 2003 The Gale Group
File 621:Gale Group New Prod.Annou.(R) 1985-2003/Oct 28
         (c) 2003 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2003/Oct 27
         (c) 2003 The Gale Group
File  16:Gale Group PROMT(R) 1990-2003/Oct 27
         (c) 2003 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 148:Gale Group Trade & Industry DB 1976-2003/Oct 28
         (c)2003 The Gale Group
File 624:McGraw-Hill Publications 1985-2003/Oct 27
         (c) 2003 McGraw-Hill Co. Inc
File  15:ABI/Inform(R) 1971-2003/Oct 28
         (c) 2003 ProQuest Info&Learning
File 647:CMP  Computer Fulltext 1988-2003/Sep W3
         (c) 2003 CMP Media, LLC
File 674:Computer News Fulltext 1989-2003/Oct W4
         (c) 2003 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2003/Oct 27
         (c) 2003 The Dialog Corp.
File 369:New Scientist 1994-2003/Oct W3
         (c) 2003 Reed Business Information Ltd.

Set     Items   Description
S1        477   (SOFT()DECISION? ? OR MAP OR (MAX OR MAXIM?)(3W)(APOSTERIO-
             R? OR A()POSTERIOR?) OR TURBO)(5N)DECOD?
S2       9066   (LOOKUP? ? OR LOOK???()UP)(3N)TABLE? ? OR LUT OR LUTS
S3        638   N(2W)(ENTRY OR ENTRIES)
S4      58439   (SECOND? OR TWO OR 2ND OR DUAL? OR MULTIPL? OR PLURAL? OR -
             SEVERAL OR VARIOUS OR DIFFERENT OR SEPARATE OR ASSORT? OR ADD-
             ITIONAL)(5N)(INDEX??? OR INDICE? ?)
S5       1298   SCALING(3N)FACTOR? ?
S6         33   S2(20N)S3:S4
S7          0   S1 AND S5 AND S6
S8       3075   TABLE? ?(20N)S3:S4
S9          0   S1 AND S8 AND S5
S10         0   S1 AND S8 AND SCAL???
S11       268   S2(20N)(INDEX?? OR INDICE? ?)
S12         0   S1 AND S11 AND S5
S13     48910   TABLE? ?(20N)(INDEX?? OR INDICE? ?)
S14         0   S1 AND S13 AND S5
S15         0   S1 AND S13 AND SCAL???
S16        29   S1 AND S2:S5
S17        18   RD (unique items)
```

17/3,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

02701267 SUPPLIER NUMBER: 99982847 (USE FORMAT 7 OR 9 FOR FULL TEXT)
DSP directory. .(Directory)(Buyers Guide)(Cover Story)
Cravotta, Robert
EDN, 48, 4, 32(13)
April 3, 2003
DOCUMENT TYPE: Buyers Guide Cover Story Directory ISSN: 0012-7515
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 10741 LINE COUNT: 00913

... billion SAD (sum of absolute differences)/sec, and as many as six MPEG-2 D1 **decodes** .

The Equator **MAP** -CA BSP (broadband-signal-processor) chip is 100% programmable in C and targets consumer applications...of buffering, provides high data throughput. The display-refresh controller provides color-space conversion, palette- **table look - up** , and hardware-cursor functions. A DES coprocessor accelerates DES encryption and decryption.

* Processor enables multiformat...

17/3,K/2 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

02647611 SUPPLIER NUMBER: 91909799 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Trade-offs exist in choice of 3G decoding scheme.
Nikolic-Popovic, Jelena
Electronic Engineering Times, 64
Sept 23, 2002
ISSN: 0192-1541 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 2119 LINE COUNT: 00173

... transmission, is widely used in wireless communications. There are several ways to accomplish Viterbi and **turbo decoding** as a component of overall symbol-rate signal processing in a basestation receiver. Each requires...

...three approaches:

- Handling all decoding in software, relying on the DSP to perform Viterbi and **turbo decoding** in addition to other processing that may be required.
- Assigning Viterbi and **turbo decoding** functions to ASICs that typically would already exist in the baseband system to handle chip...

...for the decoding function since it mostly uses instructions involving additions, subtractions, maximum searches and **table lookups** , and not multiply-accumulates like typical DSP algorithms.

The motivation for exploring the all-hardware...

...time-to-market.

One consequence of specialized hardware in this instance is that Viterbi and **turbo decoding** need to have at least partially separate hardware. Thus, the system has to be dimensioned for worst-case loading scenarios such as all users requiring Viterbi **decoding** or all users requiring **turbo decoding** . This implies that, statistically, only a portion of available resources is used at any given...

...density, as well as significantly increasing power consumption.

On-chip accelerators

The algorithm kernels for **decoding** both convolution and **turbo** codes are well defined and can therefore be implemented using "dumb" hardware, while higher levels...is freed up to perform differentiated functions rather than dumb operations nequired in Viterbi and **turbo decoding** kernels.

The disadvantages of this approach depend on the actual

implementation of the accelerator, but...
...kbits/s user takes less than 175 MHz (assuming 1.75 cycles/ butterfly), and the **turbo decoding** operation less than 225 MHz (assuming eight iterations and max-log-MAP algorithm with a...

...rate functionality for 16 (384-kbit/s) users. It would be possible to implement three **turbo decoding** channels per device rather than two, if only six iterations are performed rather than eight...

...process symbol-rate functions for 16 384-kbit/s users. The bus bandwidth required for **turbo decoding** for one channel is about 9.5 Mbits/s. Therefore, for 16 channels, 152 Mbits...

...percent, respectively.
W estimate that it takes about four man-months to implement Viterbi and **turbo decoding** in C6415 software, given the additional complexity of distributing the processing across multiple DSP devices...

17/3,K/3 (Item 3 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

02482396 SUPPLIER NUMBER: 71557070 (USE FORMAT 7 OR 9 FOR FULL TEXT)
DSP IP cores fuel PLD adoption.(Industry Trend or Event)
Mehta, Tapan A.
Electronic Engineering Times, 92
March 12, 2001
ISSN: 0192-1541 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 1898 LINE COUNT: 00160

... s, and its size varies between those of the high-speed and low-speed Viterbi **decoders** .
Turbo coding, or iterative coding, has gained considerable momentum in the past year. It is a...

...applied directly to the data and the other to an interleaved version of the data. **Turbo decoding** is iterative, and each iteration consists of decoding each convolutional code in turn. The chosen...

...To address the increasing number of opportunities in 3G applications, Altera has successfully implemented the **turbo** encoder and **decoder** at data rates in excess of 2 Mbits/s as specified by 3GPP.
The **turbo decoder** features a max-logMAP algorithm for maximum error correction and includes a 3GPP-compliant interleaver...

...Numerically controlled oscillators can be designed with DSPs, ASSPs or programmable logic. DSPs use a **lookup table** with interpolation to generate a precision sinusoid using limited on-chip SRAM. ASSPs give higher ...

17/3,K/4 (Item 4 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

02389120 SUPPLIER NUMBER: 61415741 (USE FORMAT 7 OR 9 FOR FULL TEXT)
FPGAs cranked for software radio.(Technology Information)
Dick, Chris
Electronic Engineering Times, 112
April 10, 2000
ISSN: 0192-1541 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 1850 LINE COUNT: 00156

... advanced compression algorithms, power control, channel estimation, equalization, forward error control (Viterbi, Reed-Solomon and **turbo** coding/ **decoding**) and protocol management.
Digital filters are employed in a number of ways in DSP-based...

...implemented using FPGAs. A logic element usually consists of one or more RAM n-input **lookup** **tables** , where n is between 3 and 6. There may also be additional hardware support in...

...of FPGAs. The logic elements, called slices, essentially consist of a pair of four-input **lookup** **tables** (**LUTs**), several multiplexers and some additional silicon support that allows the efficient implementation of carry-chains...
...memories. Xilinx XC4000 and Virtex devices also allow the designer to use the logic element **LUTs** as memory-either ROM or RAM. Constructing memory with this distributed-memory approach can yield...implemented using the elements that form the logic fabric-that is, the 16 x 1 **LUTs** . As an example, a 16-tap filter using 24-bit input samples and 24-bit...

17/3,K/5 (Item 5 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01673744 SUPPLIER NUMBER: 15092145 (USE FORMAT 7 OR 9 FOR FULL TEXT)
NexGen enters market with 66-MHz Nx586; first Pentium competitor uses RISC-like core and optional FPU. (Nx586 features Reduced Instruction Set Computer-like core and Floating Point Unit) (includes related article on pricing and availability of the Nx586 chip) (Product Announcement)
Gwennap, Linley
Microprocessor Report, v8, n4, p12(6)
March 28, 1994
DOCUMENT TYPE: Product Announcement ISSN: 0899-9341 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 4825 LINE COUNT: 00371

... ADD R2, R3
STORE [R1], R2
where the physical register numbers are assigned by the **decoder** to **map** the x86 registers appropriately.
Iterative x86 string instructions translate into an indefinitely long sequence of...are both four-way set-associative, further increasing the hit rate compared with Pentium's **two** -way caches. Both are physically **indexed** and tagged.
The speed of the 0.5-micron process allows accesses to occur in...

17/3,K/6 (Item 6 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01297496 SUPPLIER NUMBER: 07295278 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Making micro channel I-O easy with EPLD's. (technical)
Colleran, Tim; Webb, Michael K.; Zielke, Bob
ESD: The Electronic System Design Magazine, v19, n5, p73(6)
May, 1989
DOCUMENT TYPE: technical ISSN: 0893-2565 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2626 LINE COUNT: 00207

... applications, such as disk controllers and communications buffers. Starting and ending addresses are provided by **look - up** **tables** (**LUTs**) embedded in the part's programmable logic.
Figure-4 shows the detailed construction of the...

...has a rising edge. What value is loaded into the counters depends on the starting **LUT** . The address driver is implemented with 11 tristate primitives (CONF). When driven high by the...

... **LUT** determines the last address to be generated during the DMA cycle. TC (terminal count) goes...RD, A0, A1, and the data bus. The /CE input is created by an external **decoder** that uses address values to **map** the

EPB1400 to a specific address range. Low-order addresses--A0 and A1--are used...

17/3,K/7 (Item 7 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01037276 SUPPLIER NUMBER: 00566314
The Construction of Fast, High-Rate, Soft Decision **Block** Decoders .
Berlekamp, E.R.
IEEE Transactions on Information Theory, vIT-29, n3, p372-377
May, 1983
ISSN: 0018-9448 LANGUAGE: ENGLISH RECORD TYPE: ABSTRACT

The Construction of Fast, High-Rate, Soft Decision **Block** Decoders .

ABSTRACT: A detailed description is given of a fast **soft decision decoding** procedure for high-rate block codes. The high speed is made possible (in part) by using the symmetries of the code to simplify the syndrome decoding by **table look - up** and by making the best use of the soft decision information. The (128,106,8...

17/3,K/8 (Item 1 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

02428284 Supplier Number: 60056967 (USE FORMAT 7 FOR FULLTEXT)
Altera Introduces First Devices in Low-Cost ACEX Product Initiative.
Business Wire, p0096
March 13, 2000
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 734

... prices starting at $3.50, the ACEX 1K family offers the lowest cost of any **lookup table** -based PLD family in the market. These new devices, combined with our roadmap to a...

...PLL) and will be fully 64-bit, 66-MHz PCI-compliant. ACEX 1K devices combine **lookup tables** (**LUT**) with embedded array blocks (EABs) used to implement RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. **LUT** -based logic provides optimized performance and efficiency for datapath, mathematical, or digital signal processing (DSP...

...functions or complex logic functions, such as DSP error correction (including Reed-Solomon, Viterbi, and **Turbo** encoder/ **decoder**), wide datapath manipulation, microcontroller applications, and data-transformation functions. The combination of EABs and logic...

17/3,K/9 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

09930317 Supplier Number: 88682962 (USE FORMAT 7 FOR FULLTEXT)
A Chip on the Shoulder of Bell Labs.
McElligott, Tim
Wireless Review, pNA
June 1, 2002
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 894

... scrub. But maybe that's because so few bean counters understand the potential that a **turbo** /Viterbi **decoder** architecture - complete with a logMAP algorithm and a programmable logsum correction table - has for

driving...

...technology reduces the need to rely on a host processor and a variable width bin **lookup table**, which aides in table size correction accuracy. It is one of an increasing number of...

17/3,K/10 (Item 2 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

06549510 Supplier Number: 55393754 (USE FORMAT 7 FOR FULLTEXT)
Broadband radio developers demonstrate new concepts at Rawcon -- Designers apply advanced coding to wireless.(Industry Trend or Event)
Wirbel, Loring
Electronic Engineering Times, p22
August 9, 1999
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 1196

... can greatly improve error correction in CDMA phone systems. Honeywell uses traditional convolutional methods for **decoding** the CDMA **turbo** codes, using a soft-output Viterbi algorithm for iterative decoding at the receiver.

In optical...than hardware multipliers. Welborn said that only standard DRAM access had been studied, though the **lookup table** methodology used in the waveform storage would appear to map well into specialty memories.

Copyright...

17/3,K/11 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

15780818 SUPPLIER NUMBER: 99982847 (USE FORMAT 7 OR 9 FOR FULL TEXT)
DSP directory. (cover story).
Cravotta, Robert
EDN, 48, 4, 32(13)
April 3, 2003
ISSN: 0012-7515 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 10741 LINE COUNT: 00913

... billion SAD (sum of absolute differences)/sec, and as many as six MPEG-2 D1 **decodes**.

The Equator **MAP** -CA BSP (broadband-signal-processor) chip is 100% programmable in C and targets consumer applications...of buffering, provides high data throughput. The display-refresh controller provides color-space conversion, palette- **table look - up**, and hardware-cursor functions. A DES coprocessor accelerates DES encryption and decryption.

* Processor enables multiformat...

17/3,K/12 (Item 2 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

13214325 SUPPLIER NUMBER: 71760943 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Self-correcting codes conquer noise Part one: Viterbi codecs.(Technology Tutorial)(Tutorial)
Shah, Syed Shahzad; Yaqub, Saqib; Suleman, Faisal
EDN, 46, 4, 131
Feb 15, 2001
DOCUMENT TYPE: Tutorial ISSN: 0012-7515 LANGUAGE: English
RECORD TYPE: Fulltext
WORD COUNT: 3726 LINE COUNT: 00297

... FPGAs can realize the logic in Figure 3b by storing the hamming distances in ROM **look - up tables** . This technique minimizes the hardware required to implement a large number of branch words.

(Figure...other fast-carry schemes and using them eliminates the need to use the FPGA's **look - up table** . Hence, these units optimize both speed and size. Implementing ripple-carry adders with dedicated carry ...

...RAM. The most efficient way to implement memory in an SRAM FPGA is by using **look - up tables** . You can use them as RAMs or ROMs or for implementing combinational-logic functions. In...in a 16x1 RAM. In an SRAM-based FPGA, this implementation results in a single **look - up table** .

BIT-ERROR-RATE UNIT

"BER" (bit-error rate) refers to the number of errors in...

...ILLUSTRATION OMITTED)

When the quantization level of the demodulator output is greater than two, the **decoding** is called **soft - decision decoding** . The quantization levels are usually limited to eight (n=3 bits), because more than eight...

...4 to + 3. For hard-decision decoding the branch metric is the hamming distance; for **soft - decision decoding** , it can be the linear or Euclidean distance. The Euclidean distance for code rate, 1...

...chameleon processors are well-suited for FEC algorithms' hardware implementation. You can also implement a **soft - decision** Viterbi **decoder** in the CS2000's reconfigurable-processing fabric (Figure 10).

(Figure 10 ILLUSTRATION OMITTED)

Viterbi techniques...2/3. Error-correcting capability and hardware complexity increase as K/n decreases.

Hard-decision/ **soft - decision decoding** : The demodulator gives information to the decoder. Hard-decision decoding means that the demodulator is...

...and one. If you derive more than two quantization levels from the demodulator, then the **decoder** is **soft - decision decoding** . Hard-decision **decoding** infers a performance loss of 2 to 3 dB over **soft - decision decoding** .

Generator polynomial: A generator polynomial specifies the encoder connections. Each polynomial is of degree K...

...the received sequence and the branch word. This distance is either hamming (for hard-decision **decoding**) or Euclidean (for **soft - decision decoding**).

Path metric: An accumulation of branch metrics forms the path metric.

Trellis: The trellis diagram...

17/3,K/13 (Item 3 from file: 148)

DIALOG(R)File 148:Gale Group Trade & Industry DB

07714326 SUPPLIER NUMBER: 16682578 (USE FORMAT 7 OR 9 FOR FULL TEXT)

Gigabit DRAMs, 64-bit CPUs and more at ISSCC. (dynamic random access memory; central processing unit; International Solid State Circuits Conference) (includes related article)

Burksy, Dave

Electronic Design, v43, n4, p61(13)
Feb 20, 1995
ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 9237 LINE COUNT: 00710

... be issued or executed incorrectly due to a branch mispredict or an exception condition.

The **second** -level caches are virtually **indexed** and tagged. Each of

the specially designed cache memory chips is four-way set associative...
higher throughput. This has led some to develop application-focused DSP functions. Examples include the **Turbo** -codes encoder/ **decoder** from C.C.E.T.T., Cesson-Sevigne, France, and two MPEG-related circuits from...

17/3,K/14 (Item 4 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

07288084 SUPPLIER NUMBER: 15499151 (USE FORMAT 7 OR 9 FOR FULL TEXT)
PREP in trouble? (Programmable Electronics Performance Corp.)(includes related articles)
Parry, Simon
Electronics Weekly, n1677, p20(2)
April 20, 1994
ISSN: 0013-5224 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2053 LINE COUNT: 00159

... with across-chip routing resources. These logic cores are a mix of combinatorial logic (memory **look - up tables** , multiplexers, or AND/OR arrays) and one or more register elements. Each device's mix...bit loadable up/down binary counter.

Prescaled Counter

A 16-bit synchronous prescaled counter.

Memory **Map**

The **map decodes** address spaces ranging in size from 4K down to one. Addresses that do not correspond...

17/3,K/15 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

01255584 CMP ACCESSION NUMBER: EET20020923S0058
Trade-offs exist in choice of 3G decoding scheme
Jelena Nikolic-Popovic, Texas Instruments Canada
ELECTRONIC ENGINEERING TIMES, 2002, n 1237, PG64
PUBLICATION DATE: 020923
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Communications Design Conference
WORD COUNT: 1922

... transmission, is widely used in wireless communications. There are several ways to accomplish Viterbi and **turbo decoding** as a component of overall symbol-rate signal processing in a basestation receiver. Each requires...

...three approaches:

- Handling all decoding in software, relying on the DSP to perform Viterbi and **turbo decoding** in addition to other processing that may be required.

- Assigning Viterbi and **turbo decoding** functions to ASICs that typically would already exist in the baseband system to handle chip...
...for the decoding function since it mostly uses instructions involving additions, subtractions, maximum searches and **table lookups** , and not multiply-accumulates like typical DSP algorithms.

The motivation for exploring the all-hardware...

...time-to-market.

One consequence of specialized hardware in this instance is that Viterbi and **turbo decoding** need to have at least partially separate hardware. Thus, the system has to be dimensioned for worst-case loading

scenarios such as all users requiring Viterbi **decoding** or all users requiring **turbo decoding** . This implies that, statistically, only a portion of available resources is used at any given...

...density, as well as significantly increasing power consumption.

On-chip accelerators

The algorithm kernels for **decoding** both convolution and **turbo** codes are well defined and can therefore be implemented using "dumb" hardware, while higher levels...is freed up to perform differentiated functions rather than dumb operations nequired in Viterbi and **turbo decoding** kernels.

The disadvantages of this approach depend on the actual implementation of the accelerator, but...
...kbits /s user takes less than 175 MHz (assuming 1.75 cycles/ butterfly), and the **turbo decoding** operation less than 225 MHz (assuming eight iterations and max-log-MAP algorithm with a...

...rate functionality for 16 (384 -kbit/s) users. It would be possible to implement three **turbo decoding** channels per device rather than two, if only six iterations are performed rather than eight...

...process symbol-rate functions for 16 384- kbit/s users. The bus bandwidth required for **turbo decoding** for one channel is about 9.5 Mbits/s. Therefore, for 16 channels, 152 Mbits...

...percent, respectively.

W estimate that it takes about four man-months to implement Viterbi and **turbo decoding** in C6415 software, given the additional complexity of distributing the processing across multiple DSP devices...

17/3,K/16 (Item 2 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

01233151 CMP ACCESSION NUMBER: EET20010312S0067
DSP IP cores fuel PLD adoption
Tapan A. Mehta, Product Marketing Manager, Altera Corp., San Jose, Calif.
ELECTRONIC ENGINEERING TIMES, 2001, n 1157, PG92
PUBLICATION DATE: 010312
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: SIGNALS - FOCUS: CUSTOMIZED DSP
WORD COUNT: 1731

... s, and its size varies between those of the high-speed and low-speed Viterbi **decoders** .

Turbo coding, or iterative coding, has gained considerable momentum in the past year. It is a...

...applied directly to the data and the other to an interleaved version of the data. **Turbo decoding** is iterative, and each iteration consists of decoding each convolutional code in turn. The chosen...

...To address the increasing number of opportunities in 3G applications, Altera has successfully implemented the **turbo** encoder and **decoder** at data rates in excess of 2 Mbits/s as specified by 3GPP.

The **turbo decoder** features a max-logMAP algorithm for maximum error correction and includes a 3GPP-compliant interleaver...

...Numerically controlled oscillators can be designed with DSPs, ASSPs or programmable logic. DSPs use a **lookup table** with interpolation to

generate a precision sinusoid using limited on-chip SRAM. ASSPs give higher...

17/3,K/17   (Item 3 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

01213207   CMP ACCESSION NUMBER: EET20000410S0080
FPGAs cranked for software radio
Chris Dick, Senior System Engineer, Manager, Signal Processing Team, Xilinx Inc., San Jose, Calif.
ELECTRONIC ENGINEERING TIMES, 2000, n 1108, PG112
PUBLICATION DATE: 000410
JOURNAL CODE: EET   LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Signals - Focus: DSP World, Cores
WORD COUNT: 1690

...   advanced compression algorithms, power control, channel estimation, equalization, forward error control (Viterbi, Reed-Solomon and **turbo** coding/ **decoding**) and protocol management.

Digital filters are employed in a number of ways in DSP-based...

...implemented using FPGAs. A logic element usually consists of one or more RAM n-input **lookup tables** , where n is between 3 and 6. There may also be additional hardware support in...

...of FPGAs. The logic elements, called slices, essentially consist of a pair of four- input **lookup tables** (**LUTs**), several multiplexers and some additional silicon support that allows the efficient implementation of carry- chains...

...memories. Xilinx XC4000 and Virtex devices also allow the designer to use the logic element **LUTs** as memory-either ROM or RAM. Constructing memory with this distributed-memory approach can yield...implemented using the elements that form the logic fabric-that is, the 16 x 1 **LUTs** . As an example, a 16-tap filter using 24-bit input samples and 24-bit...

17/3,K/18   (Item 4 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

01197872   CMP ACCESSION NUMBER: EET19990809S0020
Broadband radio developers demonstrate new concepts at Rawcon - Designers apply advanced coding to wireless
Loring Wirbel
ELECTRONIC ENGINEERING TIMES, 1999, n 1073, PG22
PUBLICATION DATE: 990809
JOURNAL CODE: EET   LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: News
WORD COUNT: 1204

...   can greatly improve error correction in CDMA phone systems. Honeywell uses traditional convolutional methods for **decoding** the CDMA **turbo** codes, using a soft-output Viterbi algorithm for iterative decoding at the receiver.

In optical...than hardware multipliers. Welborn said that only standard DRAM access had been studied, though the **lookup table** methodology used in the waveform storage would appear to map well into specialty memories.

```
File   8:Ei Compendex(R) 1970-2003/Oct W3
         (c) 2003 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2003/Sep
         (c) 2003 ProQuest Info&Learning
File 202:Info. Sci. & Tech. Abs. 1966-2003/Sep 16
         (c) 2003 EBSCO Publishing
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         (c) 2003 Institution of Electrical Engineers
File  94:JICST-EPlus 1985-2003/Oct W4
         (c)2003 Japan Science and Tech Corp(JST)
File   6:NTIS 1964-2003/Oct W4
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File 144:Pascal 1973-2003/Oct W3
         (c) 2003 INIST/CNRS
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  34:SciSearch(R) Cited Ref Sci 1990-2003/Oct W3
         (c) 2003 Inst for Sci Info
File  99:Wilson Appl. Sci & Tech Abs 1983-2003/Sep
         (c) 2003 The HW Wilson Co.
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group
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File 438:Library Lit. & Info. Science 1984-2003/Sep
         (c) 2003 The HW Wilson Co
File  62:SPIN(R) 1975-2003/Sep W2
         (c) 2003 American Institute of Physics
File 239:Mathsci 1940-2003/Dec
         (c) 2003 American Mathematical Society

Set     Items   Description
S1       7549   (SOFT()DECISION? ? OR MAP OR (MAX OR MAXIM?)(3W)(APOSTERIO-
             R? OR A()POSTERIOR?) OR TURBO)(5N)DECOD?
S2      16513   (LOOKUP? ? OR LOOK???()UP)(3N)TABLE? ? OR LUT OR LUTS
S3       1121   N(2W)(ENTRY OR ENTRIES)
S4      70275   (SECOND? OR TWO OR 2ND OR DUAL? OR MULTIPL? OR PLURAL? OR -
             SEVERAL OR VARIOUS OR DIFFERENT OR SEPARATE OR ASSORT? OR ADD-
             ITIONAL)(5N)(INDEX??? OR INDICE? ?)
S5      10394   SCALING(3N)FACTOR? ?
S6         31   S2(20N)S3:S4
S7          0   S1 AND S6 AND S5
S8        662   TABLE? ?(20N)S3:S4
S9          0   S1 AND S8 AND S5
S10         0   S1 AND S8 AND SCAL???
S11       343   S2(20N)(INDEX?? OR INDICE? ?)
S12         0   S1 AND S11 AND S5
S13      8104   TABLE? ?(20N)(INDEX?? OR INDICE? ?)
S14         0   S1 AND S13 AND S5
S15         0   S1 AND S13 AND SCAL???
S16         0   S1 AND S6
S17         0   S1 AND S8
S18         2   S1 AND S13
S19        24   S1 AND S5
S20        26   S18:S19
S21        17   RD (unique items)
S22      1865   AU=(YUAN W? OR YUAN, W?)
S23         0   S1 AND S22
```

21/5/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06577686 E.I. No: EIP03437690682
Title: Implementation of a Two-Step SOVA Decoder with a Fixed Scaling Factor
Author: Kwon, Taek-Won; Choi, Jun-Rim
Corporate Source: School of Electrical Engineering Kyungpook National University, Daegu 702-701, South Korea
Source: IEICE Transactions on Communications v E86-B n 6 June 2003. p 1893-1900
Publication Year: 2003
CODEN: ITRCEC ISSN: 0916-8516
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical)
Journal Announcement: 0310W4
Abstract: Two implementation schemes for a two-step SOVA (Soft Output Viterbi Algorithm) decoder are proposed and verified in a chip. One uses the combination of trace back (TB) logic to find the survivor state and double trace back logic to find the weighting factor of a two-step SOVA. The other is that the reliability values are divided by a **scaling factor** in order to compensate for the distortion brought by overestimating those values in SOVA. We introduced a fixed **scaling factor** of 0.25 or 0.33 for a rate 1/3 and designed an 8-state **Turbo decoder** with a 256-bit frame size to lower the reliability values. The implemented architecture of the two-step SOVA decoder allows important savings in area and high-speed processing compared with the one-step SOVA decoder using register exchange (RE) or trace-back (TB) method. The chip is fabricated using 0.65mum gate array at Samsung Electronics and it shows higher SNR performance by 2 dB at the BER 10**-**4 than that of a two-step SOVA decoder without a **scaling factor** . 11 Refs.
Descriptors: *Decoding; Signal processing; Signal to noise ratio; Bit error rate; Algorithms
Identifiers: **Turbo decoders**
Classification Codes:
723.2 (Data Processing); 716.1 (Information & Communication Theory); 723.1 (Computer Programming)
723 (Computer Software, Data Handling & Applications); 716 (Electronic Equipment, Radar, Radio & Television)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATION ENGINEERING)

21/5/2 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06428436 E.I. No: EIP03277524374
Title: High performance, high throughput turbo **/SOVA** decoder **design**
Author: Wang, Zhongfeng; Parhi, Keshab K.
Corporate Source: National Semiconductor Co., Longmont, CO 80501, United States
Source: IEEE Transactions on Communications v 51 n 4 April 2003. p 570-579
Publication Year: 2003
CODEN: IECMBT ISSN: 0090-6778
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical); X; (Experimental)
Journal Announcement: 0307W1
Abstract: In this paper, two efficient approaches are proposed to improve the performance of soft-output Viterbi algorithm (SOVA)-based **turbo decoders** . In the first approach, an easily obtainable variable and a simple mapping function are used to compute a target **scaling factor** to normalize the extrinsic information output from **turbo decoders** . An extra coding gain of 0.5 dB can be obtained with additive white Gaussian noise channels. This approach does not introduce extra latency and the

hardware overhead is negligible. In the second approach, an adaptive upper bound based on the channel reliability is set for computing the metric difference between competing paths. By combining the two approaches, we show that the new SOVA-based **turbo** decoders can approach **maximum a posteriori** probability (**MAP**)-based **turbo decoders** within 0.1 dB when the target bit-error rate (BER) is moderately low (e.g., BER less than 10**-**4 for 1/2 rate codes). Following this, practical implementation issues are discussed and finite precision simulation results are provided. An area-efficient parallel decoding architecture is presented in this paper as an effective approach to design high-throughput **turbo** /SOVA **decoders** . With the efficient parallel architecture, multiple times throughput of a conventional serial decoder can be obtained by increasing the overall hardware by a small percentage. To resolve the problem of multiple memory accesses per cycle for the efficient parallel architecture, a novel two-level hierarchical interleaver architecture is proposed. Simulation results show that the proposed interleaver architecture performs as well as random interleavers, while requiring much less storage of random patterns. 35 Refs.

Descriptors: Signal theory; **Decoding** ; Algorithms; **Turbo** codes; Signal encoding; Conformal mapping; White noise; Gaussian noise (electronic); Communication channels (information theory); Probability distributions; Random processes

Identifiers: **Turbo decoder** ; Soft output Viterbi algorithm; Coding gain; Additive white Gaussian noise; **Maximum a posteriori** probability ; Parallel **decoding ; Turbo** interleaver

Classification Codes:

716.1 (Information & Communication Theory); 723.2 (Data Processing); 922.1 (Probability Theory)

716 (Electronic Equipment, Radar, Radio & Television); 723 (Computer Software, Data Handling & Applications); 922 (Statistical Methods)

71 (ELECTRONICS & COMMUNICATION ENGINEERING); 72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

21/5/3 (Item 3 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

06413725 E.I. No: EIP03247505752

Title: A simplified and efficient implementation of FPGA-based turbo decoder

Author: Sharma, Sanjay; Attri, Sanjay; Chauhan, R.C.

Corporate Source: Department of ECE SLIET, Longowal, Sangrur, Punjab, India

Conference Title: 22nd IEEE International Performance, Computing, and Communications Conference

Conference Location: Phoenix, AZ, United States Conference Date: 20030409-20030411

Sponsor: IEEE Computer Society; IEEE Computer Society Technical Committee on the Internet; IEEE Communications Society

E.I. Conference No.: 61065

Source: IEEE International Performance, Computing and Communications Conference, Proceedings 2003. p 207-213 (IEEE cat n 03CH37463)

Publication Year: 2003

Language: English

Document Type: CA; (Conference Article) Treatment: A; (Applications); T ; (Theoretical); X; (Experimental)

Journal Announcement: 0306W4

Abstract: In the Max-Log- **MAP decoding** algorithm, the branch metrics are modified by weighting a-priori values by a suitable **scaling factor** , resulting in a significant BER improvement. Using Integer arithmetic and proper hardware management, an efficient implementation of a **Turbo Decoder** based on the modified form of Max-Log-MAP algorithm is proposed. All internal metrics are represented and operated on integers, avoiding complex calculation seen in floating and fixed-point arithmetic. **Turbo Decoder** is implemented by a careful manipulation of the hardware with a single decoder structure without any interleaving and deinterleaving delay, resulting high data throughput with very low FPGA resource utilization.

The final FPGA design consumes approximately 695mW to achieve throughput of more than 1 Mbps with eight iterations. With channel inputs of only 3 bits (8 levels), the integer version of **Turbo Decoder** results in less than 0.5dB loss of E//bN//o from the optimal floating point **Turbo Decoder** . 13 Refs.

Descriptors: *Decoding; Field programmable gate arrays; Bit error rate; Computer hardware; Communication channels (information theory); Application specific integrated circuits; Algorithms; Computer architecture; Code division multiple access; Signal to noise ratio; Digital arithmetic

Identifiers: **Turbo decoder** ; Metric normalization; Sub-block processing

Classification Codes:

723.2 (Data Processing); 721.2 (Logic Elements); 723.1 (Computer Programming); 716.1 (Information & Communication Theory); 721.1 (Computer Theory (Includes Formal Logic, Automata Theory, Switching Theory & Programming Theory))

723 (Computer Software, Data Handling & Applications); 721 (Computer Circuits & Logic Elements); 716 (Electronic Equipment, Radar, Radio & Television)

72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATION ENGINEERING)

21/5/4 (Item 4 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

05843613 E.I. No: EIP01266559722

Title: A study on the performance, complexity tradeoffs of block turbo decoder **design**

Author: Chi, Z.; Song, L.; Parhi, K.K.

Corporate Source: Dept. of Elect. and Comp. Eng. University of Minnesota, Minneapolis, MN 55455, United States

Conference Title: Thermoelectric Materials 2000-The Next Generation Materials for Small-Scale Refrigeration and Power Generation Applications

Conference Location: San Francisco, CA, United States Conference Date: 20000424-20000427

E.I. Conference No.: 58143

Source: Materials Research Society Symposium - Proceedings v 626 2001. p IV65-IV68

Publication Year: 2001

CODEN: MRSPDH ISSN: 0272-9172

Language: English

Document Type: CA; (Conference Article) Treatment: T; (Theoretical)

Journal Announcement: 0107W1

Abstract: In this paper, results from a study of the tradeoffs between VLSI implementation complexity and performance of block **turbo decoder** are presented. Specifically, we address low complexity design strategies on choosing the **scaling factor** of the log extrinsic information, reducing the number of hard decision decodings and reducing the complexity of general hard-decision BCH **decoders** when **soft - decision decodings** are utilized. 11 Refs.

Descriptors: **Decoding ; Turbo codes** ; VLSI circuits; Bit error rate; Optical communication; Data transfer

Identifiers: Block **turbo decoder**

Classification Codes:

723.2 (Data Processing); 714.2 (Semiconductor Devices & Integrated Circuits); 723.1 (Computer Programming); 717.1 (Optical Communication Systems)

723 (Computer Software, Data Handling & Applications); 714 (Electronic Components & Tubes); 717 (Electro-Optical Communication)

72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATION ENGINEERING)

21/5/5 (Item 5 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

05753376 E.I. No: EIP01015471353

Title: Optimal Turbo decoding **metric generation in a pilot assisted coherent wireless communication system**

Author: Ling, Fuyun

Corporate Source: Qualcomm Inc, San Diego, CA, USA

Conference Title: 52nd Vehicular Technology Conference (IEEE VTS Fall VTC2000)

Conference Location: Boston, MA, USA Conference Date: 20000924-20000928

Sponsor: IEEE Boston Section; IEEE Vehicular Technology Society

E.I. Conference No.: 57805

Source: IEEE Vehicular Technology Conference v 1 n 52ND 2000. IEEE, Piscataway, NJ, USA,00CB37152. p 298-302

Publication Year: 2000

CODEN: IVTCDZ ISSN: 0740-0551

Language: English

Document Type: CA; (Conference Article) Treatment: T; (Theoretical)

Journal Announcement: 0102W3

Abstract: In this paper, we derive the exact expressions of the log-likelihood ratio (LLR) values generated from coherent demodulation using the channel coefficient estimated based on the pilot signal. These results are obtained based on the analytical results given in left bracket 1 right bracket . It is shown that for Rayleigh fading channels, the LLR values for **Turbo decoding** are the scaled dot products of the channel estimate and the sample of the coded bits. Examples of the computation of the LLR values are given. Considerations and principles for practical implementations are discussed. Simulation results are provided to demonstrate the importance of choosing the proper **scaling factor** in achieving optimal decoding performance. (Author abstract) 5 Refs.

Descriptors: *Wireless telecommunication systems; Communication channels (information theory); Rayleigh fading; Demodulation; Decoding; Signal encoding; Error analysis; Error correction; Coding errors; Computer simulation

Identifiers: Log-likelihood ratio (LLR) values; Turbo codes; Pilot signals

Classification Codes:

716.1 (Information & Communication Theory); 716.3 (Radio Systems & Equipment); 713.3 (Modulators, Demodulators, Limiters, Discriminators, Mixers); 921.6 (Numerical Methods); 723.2 (Data Processing)

716 (Radar, Radio & TV Electronic Equipment); 713 (Electronic Circuits) ; 921 (Applied Mathematics); 723 (Computer Software)

71 (ELECTRONICS & COMMUNICATIONS); 92 (ENGINEERING MATHEMATICS); 72 (COMPUTERS & DATA PROCESSING)

21/5/6 (Item 6 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

05725576 E.I. No: EIP00125433816

Title: Improving the max-log- MAP turbo decoder

Author: Vogt, J.; Finger, A.

Corporate Source: Dresden Univ of Technology, Dresden, Ger

Source: Electronics Letters v 36 n 23 Nov 2000. p 1937-1939

Publication Year: 2000

CODEN: ELLEAK ISSN: 0013-5194

Language: English

Document Type: JA; (Journal Article) Treatment: T; (Theoretical)

Journal Announcement: 0101W4

Abstract: **Decoding turbo** codes with the max-log-MAP algorithm is a good compromise between performance and complexity. The **decoding** quality of the max-log- **MAP decoder** is improved by using a **scaling factor** within the extrinsic calculation. Simulations using the IMT-2000/3GPP parameters demonstrate that this method gives approximately 0.2 to 0.4 dB performance gain compared to the standard max-log-MAP algorithm. (Author abstract) 7 Refs.

Descriptors: *Decoding; Algorithms; Gain measurement; Signal to noise ratio; Iterative methods; Codes (symbols); Computer simulation; Rayleigh

fading; Computational complexity
Identifiers: **Turbo decoders**
Classification Codes:
723.2 (Data Processing); 716.1 (Information & Communication Theory); 942.2 (Electric Variables Measurements); 921.6 (Numerical Methods); 723.5 (Computer Applications)
723 (Computer Software); 716 (Radar, Radio & TV Electronic Equipment); 921 (Applied Mathematics); 942 (Electrical & Electronic Measuring Instruments)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS); 92 (ENGINEERING MATHEMATICS); 94 (INSTRUMENTS & MEASUREMENT)

21/5/7 (Item 7 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05670988 E.I. No: EIP00105353494
Title: Efficient approaches to improving performance of VLSI SOVA-based Turbo decoders
Author: Wang, Zhongfeng; Suzuki, Hiroshi; Parhi, Keshab K.
Corporate Source: Univ of Minnesota, Minneapolis, MN, USA
Conference Title: Proceedings of the IEEE 2000 Internaitonal Symposium on Circuits and Systems
Conference Location: Geneva, Switz Conference Date: 19000528-19000531
Sponsor: IEEE Circuits and Systems Society
E.I. Conference No.: 57398
Source: Proceedings - IEEE International Symposium on Circuits and Systems v 1 2000. IEEE, Piscataway, NJ, USA,00CB36353. p I-287-I-290
Publication Year: 2000
CODEN: PICSDI ISSN: 0271-4310
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 0011W3
Abstract: In this paper, we propose two VLSI applicable approaches to improving performance of soft-output Viterbi algorithm (SOVA)-based **Turbo decoders** . In the first approach, a pseudo-median filter is employed to modify the soft outputs of each SOVA-based constituent **decoder** . Compared with conventional SOVA-based **Turbo decoders** , an extra coding gain of 0.2 dB can be achieved for a wide range of target bit-error-rate (BER). In the second approach, an easily obtainable variable and a simple mapping function are used to avoid the complex computation of the **scaling factor** for extrinsic information in SOVA-based **Turbo decoders** . An extra coding gain of 0.3 to 0.5 dB can be obtained in general. This approach does not require signal-to-noise ratio (SNR) related information while the original method does. The hardware overhead and the extra latency for both approaches are negligible. (Author abstract) 11 Refs.
Descriptors: *Decoding; VLSI circuits; Algorithms; Electric filters; Bit error rate; Signal to noise ratio; Functions
Identifiers: Soft output Viterbi algorithm; Turbo codes; Simple mapping functions
Classification Codes:
723.2 (Data Processing); 714.2 (Semiconductor Devices & Integrated Circuits); 703.2 (Electric Filters); 723.1 (Computer Programming)
723 (Computer Software); 714 (Electronic Components); 921 (Applied Mathematics); 703 (Electric Circuits)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS); 92 (ENGINEERING MATHEMATICS); 70 (ELECTRICAL ENGINEERING)

21/5/8 (Item 8 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05670347 E.I. No: EIP00105352851
Title: Modified two-step SOVA-based turbo decoder **with a fixed** scaling factor
Author: Kim, Dae Won; Kwon, Taek Won; Choi, Jun Rim; Kong, Jun Jin

Corporate Source: Kyungpook Natl Univ, Taegu, South Korea
Conference Title: Proceedings of the IEEE 2000 Internaitonal Symposium on Circuits and Systems
Conference Location: Geneva, Switz   Conference Date: 19000528-19000531
Sponsor: IEEE Circuits Systems Society
E.I. Conference No.: 57401
Source: Proceedings - IEEE International Symposium on Circuits and Systems v 4 2000. IEEE, Piscataway, NJ, USA,00CB36353. p IV-37-IV-40
Publication Year: 2000
CODEN: PICSDI   ISSN: 0271-4310
Language: English
Document Type: CA; (Conference Article)   Treatment: T; (Theoretical)
Journal Announcement: 0011W3
Abstract: In this paper, two optimum implementation schemes are proposed in soft output Viterbi algorithm (SOVA) with high performance. One is modifying the architecture known as two-step SOVA scheme in order to obtain high speed. The other is lowering the reliability values to a same level with a **scaling factor** 0.25 or 0.33 for hardware implementation in order to compensate for the distortion. Also, we have implemented one step SOVA and the modified architecture for comparison of two schemes with 0.65 um Samsung SOG technology using verilog HDL. At result, The modified architecture provides higher SNR performance by 2 dB at the BER 1E-04 than that of the general SOVA. Also we have obtained good performance by using a fixed **scaling factor** , by which the soft output of SOVA can be considered as being multiplied. The simulation results show that the modified architecture with both methods contributes to high performance. (Author abstract) 5 Refs.
Descriptors: *Image coding; Convolutional codes; Decoding; Algorithms; Computer simulation; Signal to noise ratio
Identifiers: Turbo codes; Soft output Viterbi algorithm
Classification Codes:
723.2 (Data Processing); 723.1 (Computer Programming); 723.5 (Computer Applications)
741 (Optics & Optical Devices); 723 (Computer Software); 921 (Applied Mathematics)
74 (OPTICAL TECHNOLOGY); 72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

21/5/10   (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

7702451   INSPEC Abstract Number: B2003-09-6120B-023
Title: Implementation of turbo decoder **based on two-step SOVA with a** scaling factor
Author(s): Dae Won Kim; Jun Rim Choi
Author Affiliation: Sch. of Electr. Eng. & Comput. Sci., Kyungpook Nat. Univ., South Korea
Journal: Journal of the Institute of Electronics Engineers of Korea SD vol.39-SD, no.11   p.14-23
Publisher: Inst. Electron. Eng. Korea,
Publication Date: Nov. 2002 Country of Publication: South Korea
ISSN: 1229-6368
SICI: 1229-6368(200211)39SD:11L.14:ITDB;1-6
Material Identity Number: N510-2003-001
Language: Korean   Document Type: Journal Paper (JP)
Treatment: Practical (P); Theoretical (T); Experimental (X)
Abstract: Two implementation methods for SOVA (soft output Viterbi algorithm) of **turbo decoder** are applied and verified. The first method is the combination of a trace back (TB) logic for the survivor state and a double trace back logic for the weight value in two-step SOVA. This architecture of two-step SOVA decoder allows important savings in area and high-speed processing compared with that of one-step SOVA decoding using register exchange (RE) or trace-back (TB) method. Second method is adjusting the reliability value with a **scaling factor** between 0.25 and 0.33 in order to compensate for the distortion for a rate 1/3 and 8-state SOVA decoder with a 256-bit frame size. The proposed schemes contributed to

higher SNR performance by 2dB at the BER 10E-4 than that of SOVA decoder without a **scaling factor** . In order to verify the suggested schemes, the SOVA decoder is tested using Xilinx XCV 1000E FPGA, which runs at 33.6MHz of the maximum speed with 845 latencies and it features 175K gates in the case of 256-bit frame size. (14 Refs)

Subfile: B

Descriptors: field programmable gate arrays; turbo codes; Viterbi decoding

Identifiers: **turbo decoder** ; two-step SOVA; **scaling factor** ; trace back logic; survivor state; double trace back logic; weight value; area; high-speed processing; reliability value; frame size; SNR performance; Xilinx XCV 1000E FPGA; latencies; soft output Viterbi algorithm; 33.6 MHz; 256 bit

Class Codes: B6120B (Codes)

Numerical Indexing: frequency 3.36E+07 Hz; word length 2.56E+02 bit

21/5/12 (Item 4 from file: 2)

DIALOG(R)File 2:INSPEC

7354867 INSPEC Abstract Number: B2002-09-6120B-072, C2002-09-5210B-068

Title: VLSI implementation for low density parity check decoder

Author(s): Lee, W.L.; Wu, A.; Li, P.

Author Affiliation: Dept. of Electron. Eng., City Polytech. of Hong Kong, Kowloon, China

Conference Title: ISIC-2001. 9th International Symposium on Integrated Circuits, Devices and Systems. Proceedings. Low Power and Low Voltage Integrated Systems p.250-3

Publisher: Nanyang Technol. Univ, Singapore

Publication Date: 2001 Country of Publication: Singapore ix+503 pp.

Material Identity Number: XX-2001-01094

Conference Title: Proceedings of 9th International Symposium on Integrated Circuits, Devices and Systems

Conference Sponsor: Celestry Design Technol

Conference Date: 3-5 Sept. 2001 Conference Location: Singapore

Language: English Document Type: Conference Paper (PA)

Treatment: Applications (A); Practical (P); Theoretical (T)

Abstract: In this paper, a low complexity digital low density parity check (LDPC) **turbo** code **decoder** architecture for real-time cellular personal communication application is presented. The proposed VLSI decoder architecture alleviates the use of complex operations such as combinational arithmetic, exponent computations and reduces intermediate storage as well as interleaving latency by incorporating in-place algorithm, **index** look-up **table** and address counter. Besides, output section and termination of iteration are implemented by simple decision logic. The entire decoder is designed and synthesized using Synopsys VHDL computer aided design tool. (8 Refs)

Subfile: B C

Descriptors: decoding; hardware description languages; integrated circuit design; table lookup; turbo codes; VLSI

Identifiers: VLSI; low density parity check decoder; turbo code; decoder architecture; intermediate storage; in-place algorithm; **index** look-up **table** ; address counter; output section; decision logic; Synopsys; VHDL; computer aided design tool; interleaving; latency; real-time cellular personal communication application; combinational arithmetic; exponent computations

Class Codes: B6120B (Codes); B1265A (Digital circuit design, modelling and testing); B2570A (Semiconductor integrated circuit design, layout, modelling and testing); B1130B (Computer-aided circuit analysis and design) ; C5210B (Computer-aided logic design); C7410D (Electronic engineering computing)

21/5/14 (Item 6 from file: 2)

DIALOG(R)File 2:INSPEC

6874037 INSPEC Abstract Number: B2001-04-6250F-283
Title: Optimal turbo decoding **metric generation in a pilot assisted coherent wireless communication system**
Author(s): Fuyun Ling
Author Affiliation: Qualcomm Inc., San Diego, CA, USA
Conference Title: Vehicular Technology Conference Fall 2000. IEEE VTS Fall VTC2000. 52nd Vehicular Technology Conference (Cat. No.00CH37152) Part vol.1 p.298-302 vol.1
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA 6 vol. 3040 pp.
ISBN: 0 7803 6507 0 Material Identity Number: XX-2000-02562
U.S. Copyright Clearance Center Code: 0 7803 6507 0/2000/$10.00
Conference Title: Vehicular Technology Conference Fall 2000. IEEE VTS Fall VTC2000. 52nd Vehicular Technology Conference
Conference Sponsor: IEEE Boston Sect.; IEEE Vehicular Technol. Soc
Conference Date: 24-28 Sept. 2000 Conference Location: Boston, MA, USA
Medium: Also available on CD-ROM in PDF format
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: In this paper, we derive the exact expressions of the log-likelihood ratio (LLR) values generated from coherent demodulation using the channel coefficient estimated based on the pilot signal. These results are obtained based on the analytical results given in Ling (1999). It is shown that for Rayleigh fading channels, the LLR values for **turbo decoding** are the scaled dot products of the channel estimate and the sample of the coded bits. Examples of the computation of the LLR values are given. Considerations and principles for practical implementations are discussed. Simulation results are provided to demonstrate the importance of choosing the proper **scaling factor** in achieving optimal decoding performance. (5 Refs)
Subfile: B
Descriptors: channel coding; decoding; demodulation; land mobile radio; Rayleigh channels; turbo codes
Identifiers: optimal **turbo decoding** metric generation; pilot assisted coherent wireless communication system; log-likelihood ratio; coherent demodulation; channel coefficient; Rayleigh fading channels; LLR values; scaled dot products; **scaling factor** ; mobile radio
Class Codes: B6250F (Mobile radio systems); B6120B (Codes)

21/5/17 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

6514428 INSPEC Abstract Number: B2000-04-6120B-047
Title: A modified two-step SOVA-based turbo decoder **for low power and high performance**
Author(s): Taek Won Kwon; Dae Won Kim; Woo Tae Kim; Eon Kyeong Joo; Jun Rim Choi; Pyung Choi; Jun Jin Kong; Sung Han Choi; Won Hee Chung; Ki Won Lee
Author Affiliation: Sch. of Electron. & Electr. Eng., Kyungpook Nat. Univ., Taegu, South Korea
Conference Title: Proceedings of IEEE. IEEE Region 10 Conference. TENCON 99. `Multimedia Technology for Asia-Pacific Information Infrastructure' (Cat. No.99CH37030) Part vol.1 p.297-300 vol.1
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1999 Country of Publication: USA 2 vol.xxxvii+1583 pp.
ISBN: 0 7803 5739 6 Material Identity Number: XX-2000-00012
U.S. Copyright Clearance Center Code: 0 7803 5739 6/99/$10.00
Conference Title: Proceedings of IEEE. IEEE Region 10 Conference. TENCON 99. `Multimedia Technology for Asia-Pacific Information Infrastructure'
Conference Sponsor: Inst. Electron Eng. Korea; Korea Inf. Sci. Soc.; Korean Inst. Electr. Eng.; Korean Inst. Commun. Sci.; IEEE Region 10; Minist. Sci. & Technol.; Minist. Educ.; Cheju Province

Conference Date: 15-17 Sept. 1999 Conference Location: Cheju Island, South Korea
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Theoretical (T)
Abstract: In this paper two methods for low power and high performance are proposed for the soft output Viterbi algorithm (SOVA). One is to employ a modified architecture using a combination of a trace back (TB) for finding survivor states and a double trace back for finding the weight in two-step SOVA. The other is to lower the reliability values to the same level as a **scaling factor** to compensate for the distortion brought by overestimating those values in the original SOVA. We introduce a fixed **scaling factor** 0.25 or 0.33 for a rate 1/3 and 8-state **turbo decoder** with a 256-bit frame in hardware implementation to lower the reliability values. The modified architecture used in two-step SOYA allows important savings in area and power dissipation, compared with those of one-step (register exchange (RE) or TB) SOVA, and it also provides higher SNR performance (2 dB at the BER IE-04) than that of the conventional SOVA. Good performance is obtained by using a fixed **scaling factor** by which the soft output of SOVA can be considered as being multiplied. The simulation results show that the modified architecture with both methods contributes to low power and high performance. (5 Refs)
Subfile: B
Descriptors: error statistics; turbo codes; Viterbi decoding
Identifiers: SOVA; **turbo decoder** ; soft output Viterbi algorithm; trace back; double trace back; low power; high performance; two-step SOVA; fixed **scaling factor** ; SNR performance; BER; simulation results; modified architecture
Class Codes: B6120B (Codes)

Search Results

Search Results for: **[scaling factor*<AND>((table* <near/20> (index* or indice*) <AND>(((soft decision* or map or maximum a-posterior* or maximum aposterior* or turbo) <near/5> decod*))))]**
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1 Direct volume rendering with shading via three-dimensional textures 77%
Allen Van Gelder , Kwansik Kim
Proceedings of the 1996 symposium on Volume visualization October 1996

Results 1 - 1 of 1 short listing